

PHRAA

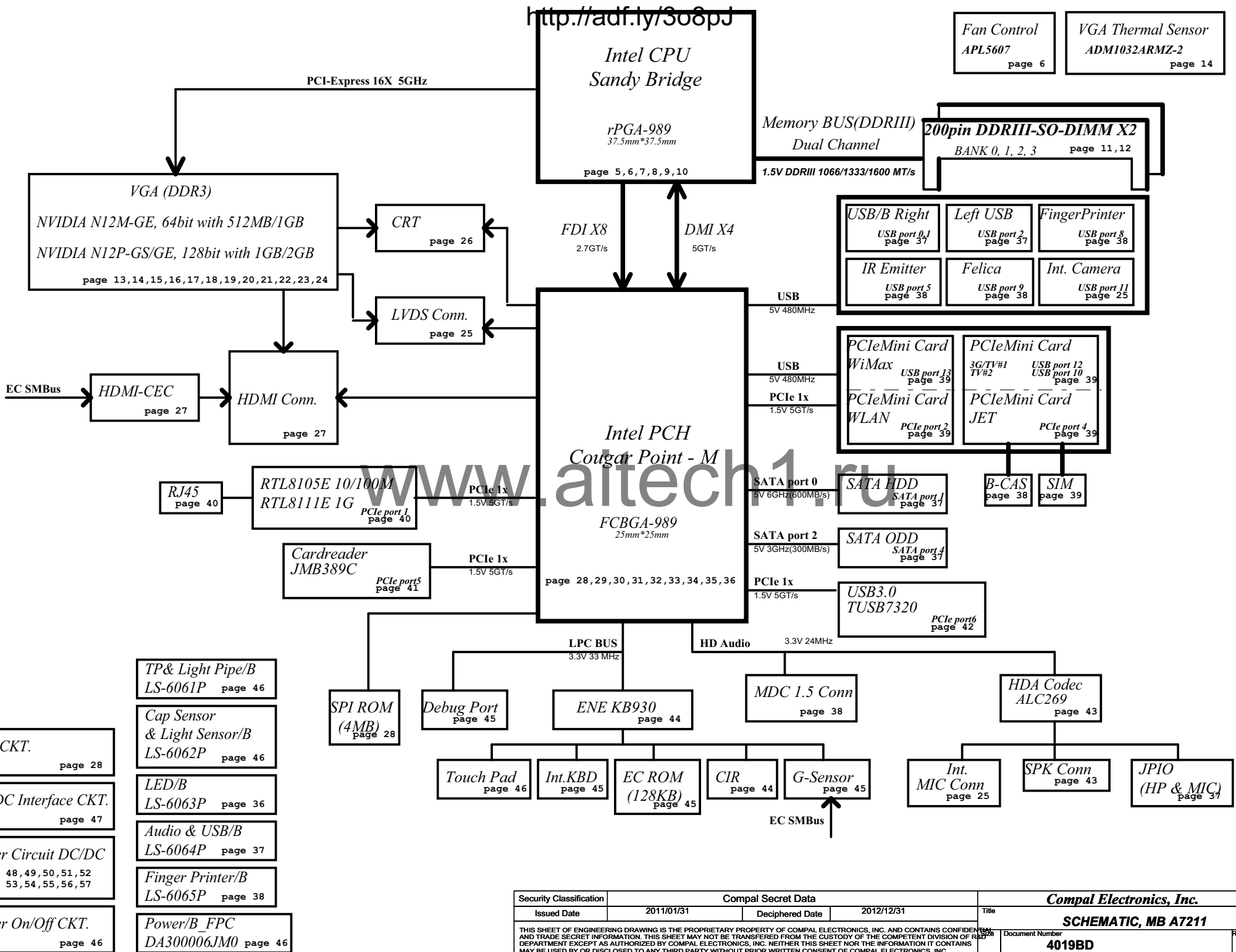
Superior 10/10G

LA-7211P REV 1.0 Schematic

Intel Processor(Sandy Bridge) / PCH(Cougar Point)
2011-01-31 Rev 1.0

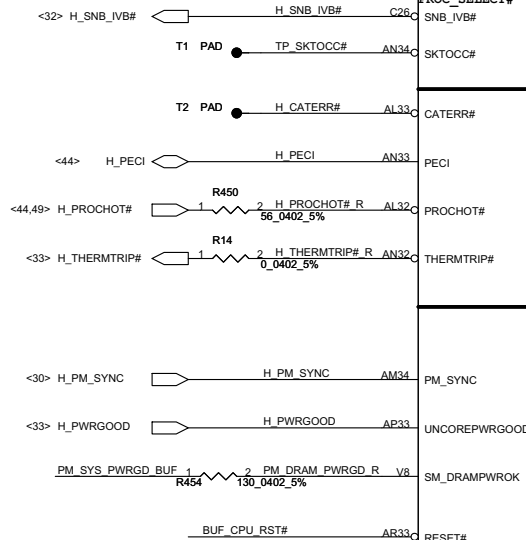
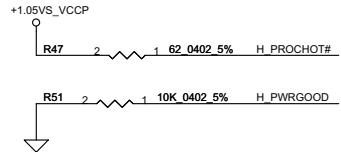
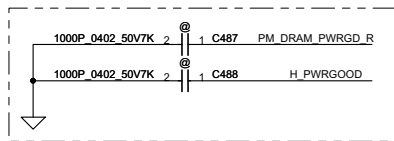
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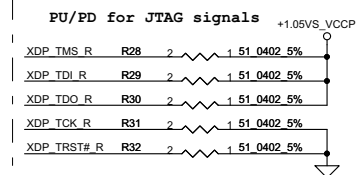
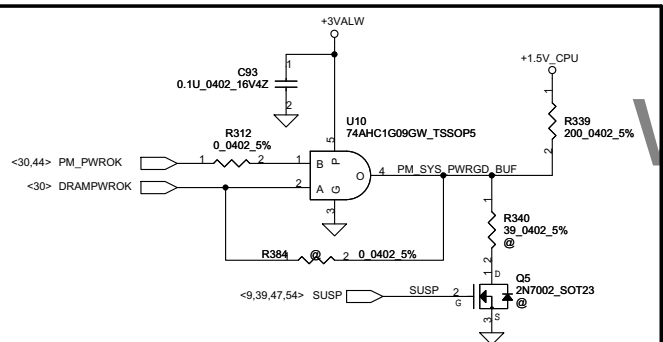
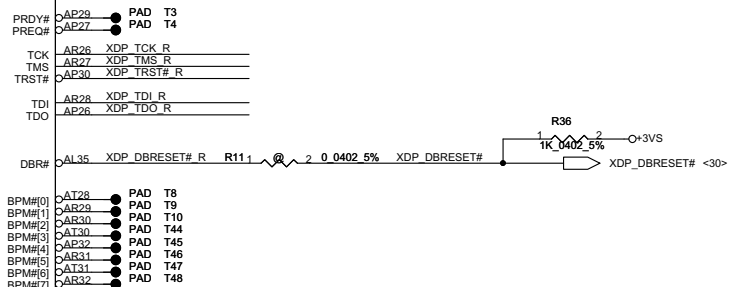
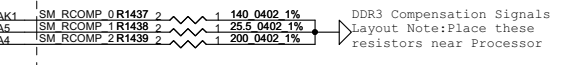
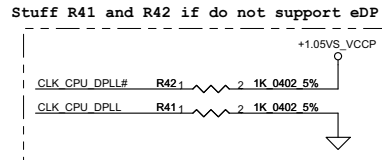
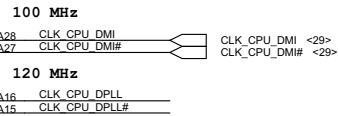
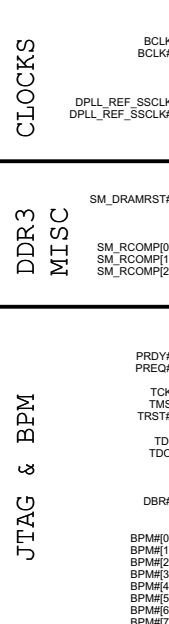


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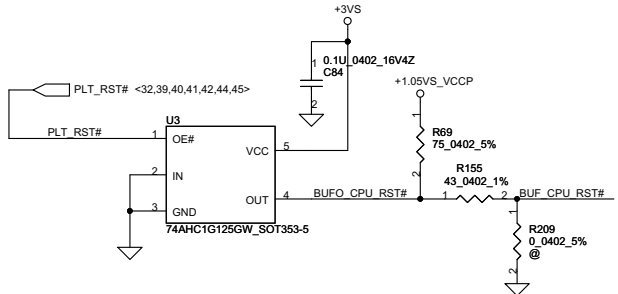
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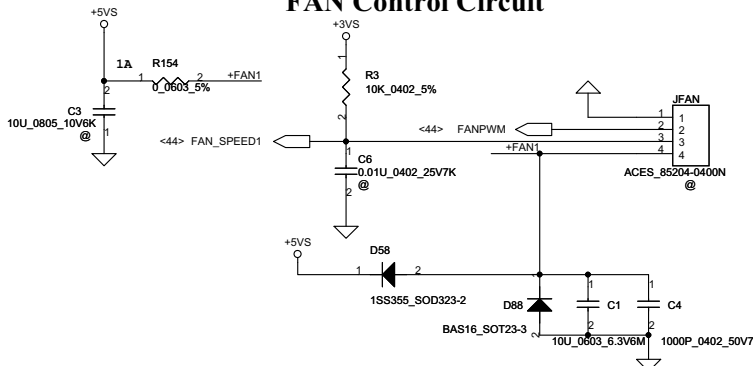
Sandy Bridge_rPGA_Rev0p61



Buffered Reset to CPU

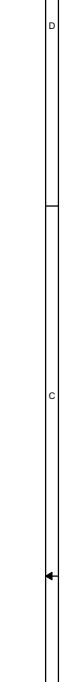
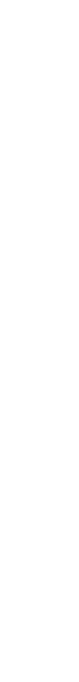
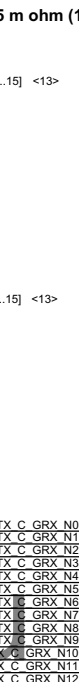
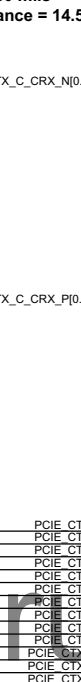
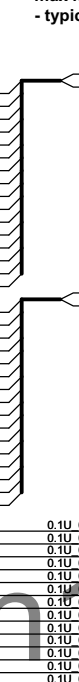
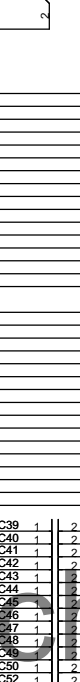
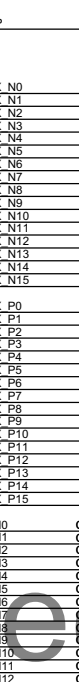
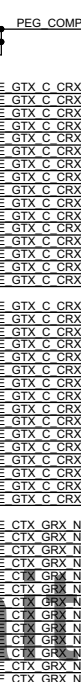
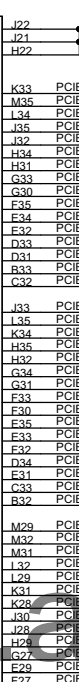
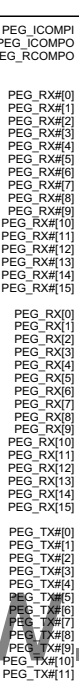
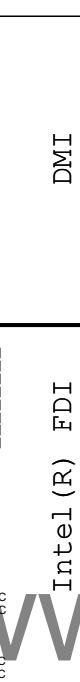
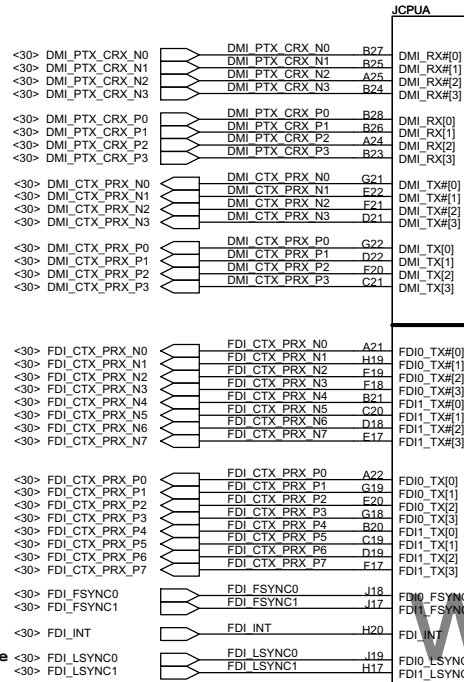


FAN Control Circuit



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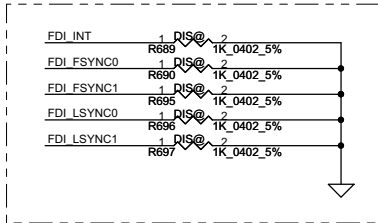
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)



eDP_COMP signals should be shorted near balls and routed with typical impedance <25m ohm



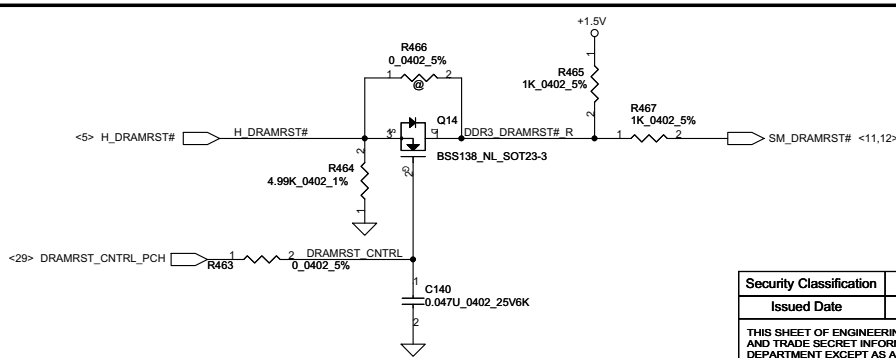
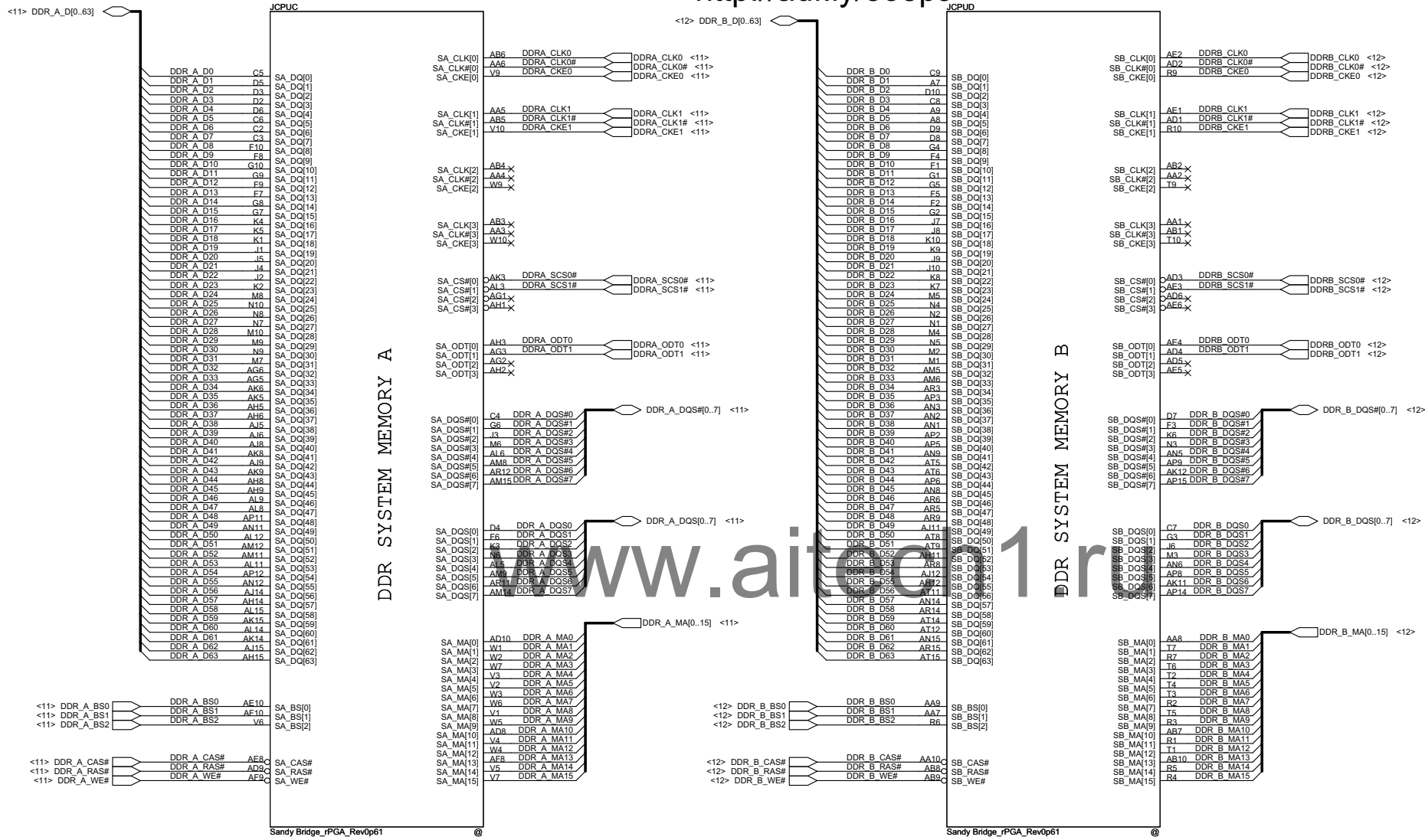
Close to CPU



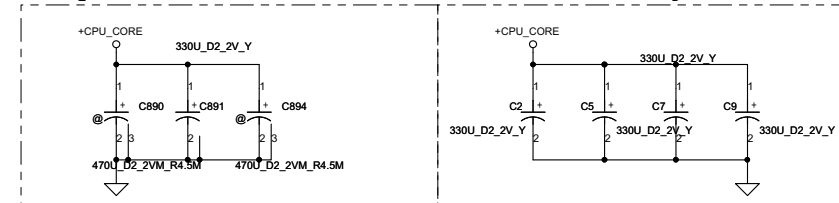
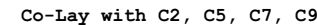
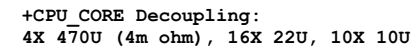
Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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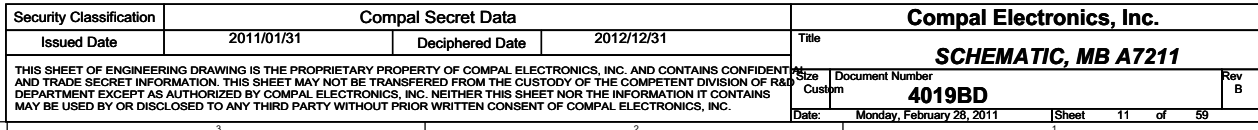


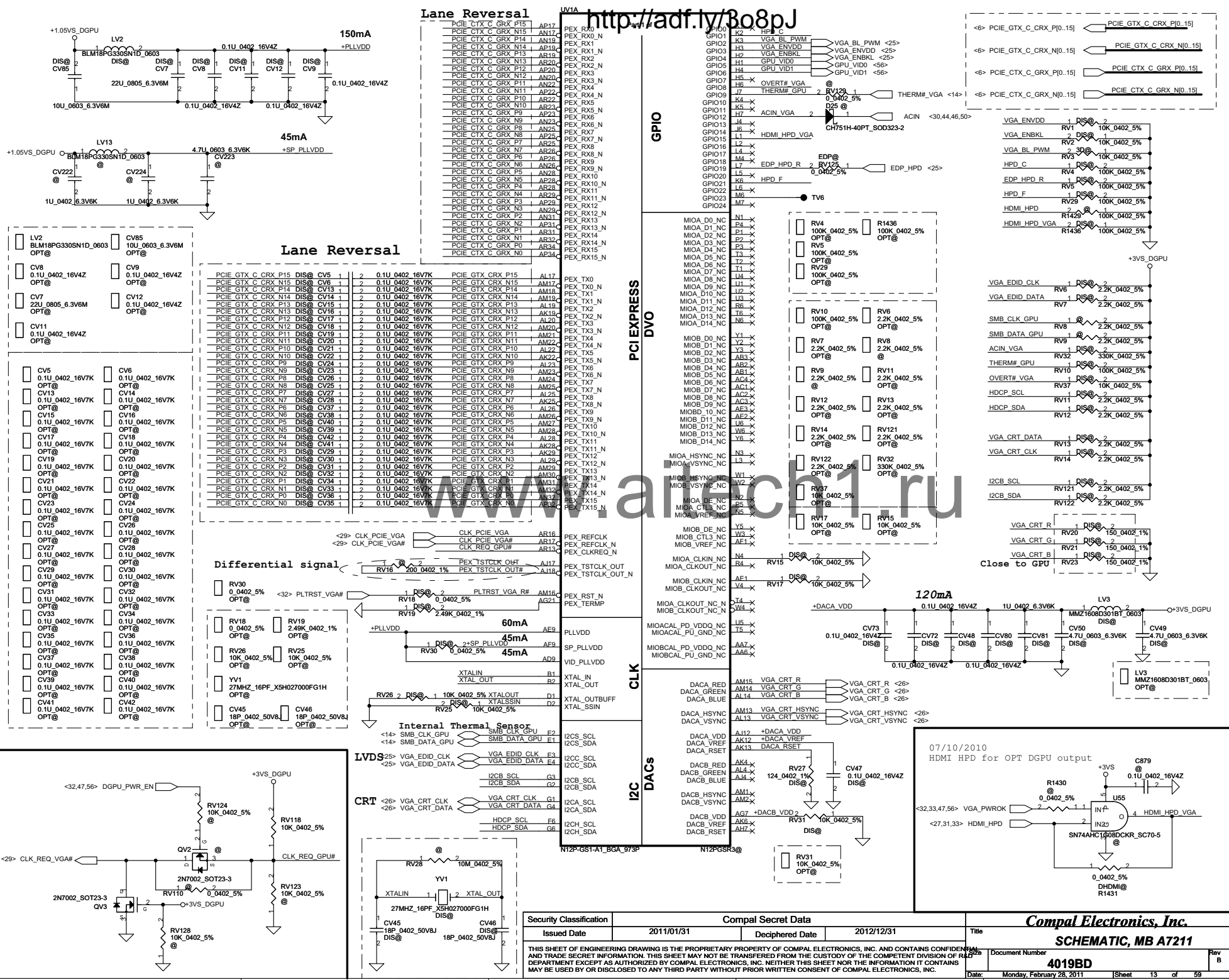
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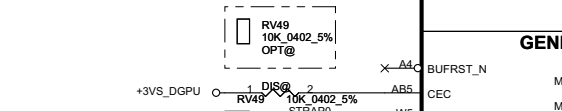
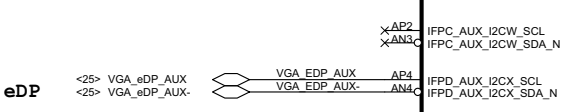
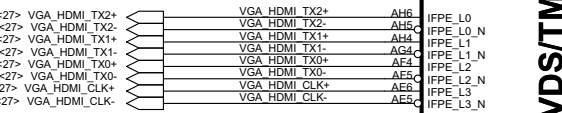
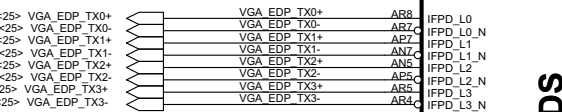
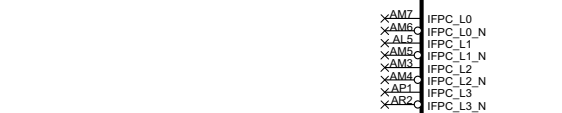
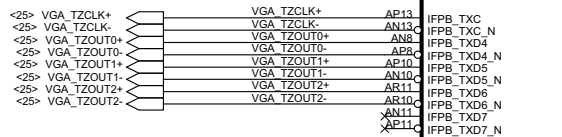
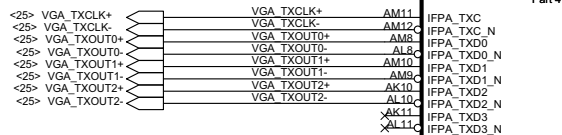
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NC

LVDS/TMDS

TEST

TESTMODE

SERIAL

GENERAL

NC/SPDIF_NC

MULTI_STRAP_REF0_GND

MULTI_STRAP_REF1_GND

THERMDP

THERMDN

NC/SPDIF_NC

MULTI_STRAP_REF0_GND

MULTI_STRAP_REF1_GND

THERMDP

THERMDN

NC/SPDIF_NC

MULTI_STRAP_REF0_GND

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THERMDP

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MULTI_STRAP_REF0_GND

MULTI_STRAP_REF1_GND

THERMDP

THERMDN

NC/SPDIF_NC

MULTI_STRAP_REF0_GND

For PHQAA EVT Phase only

Mode	VID1	VID0	+VGA_CORE
P0 (Cold)	1	1	0.95 V
P0	0	1	0.950V
P8/P12	0	0	0.825 V

N12M-GE Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	606	790	1.00 V
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

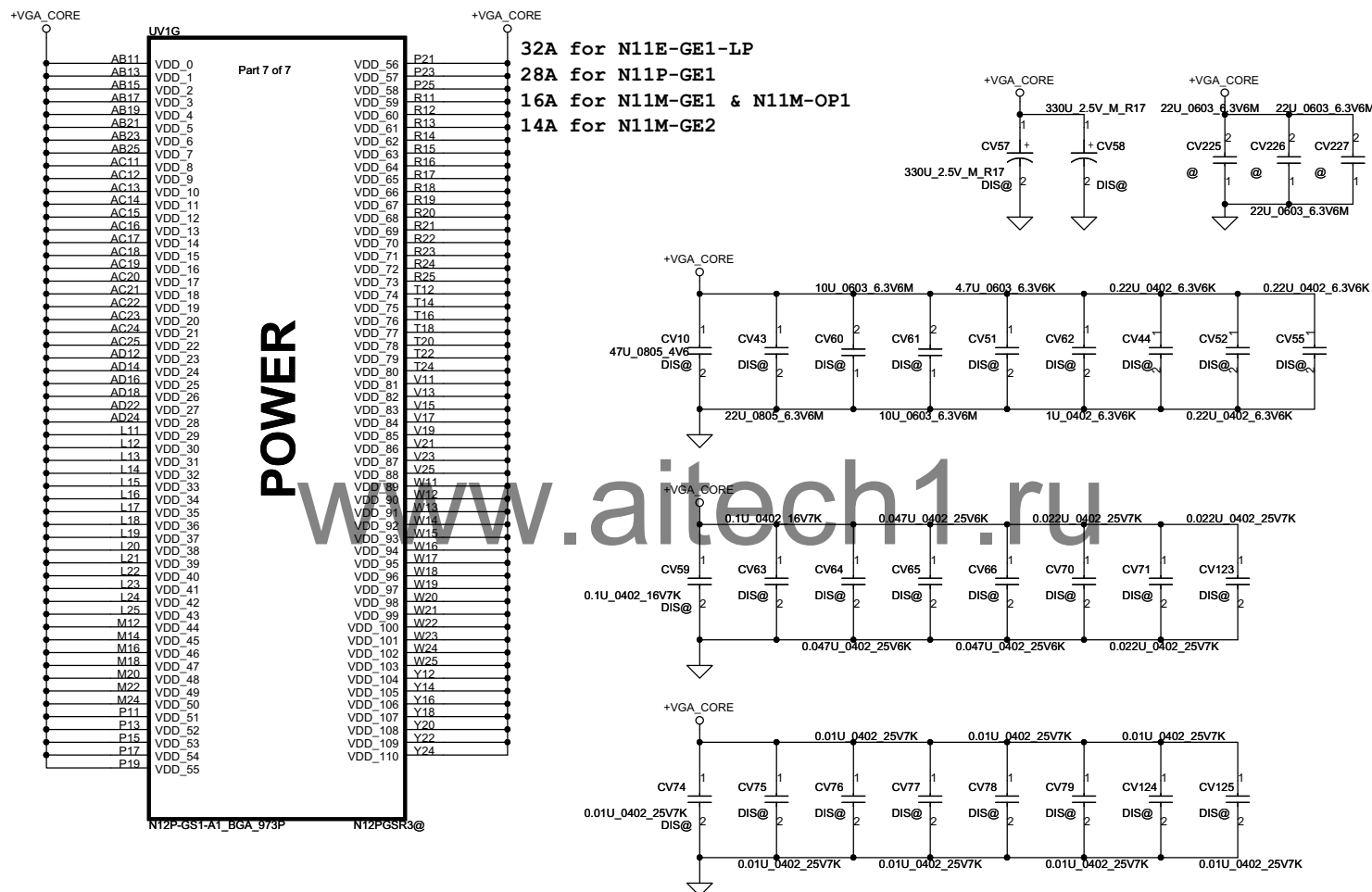
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N12P-GE Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD

N12P-GE Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0	TBD	TBD	TBD
P8	TBD	TBD	TBD
P12	TBD	TBD	TBD



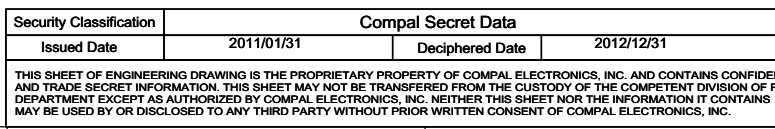




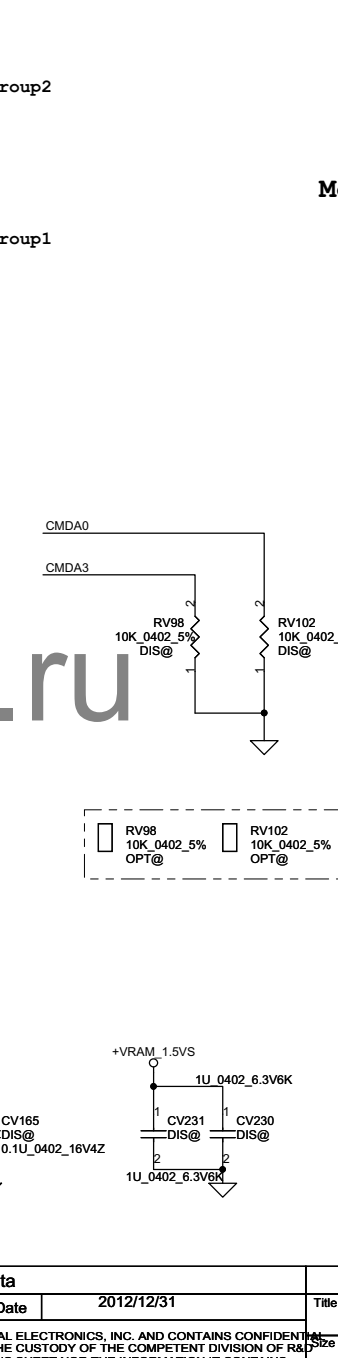
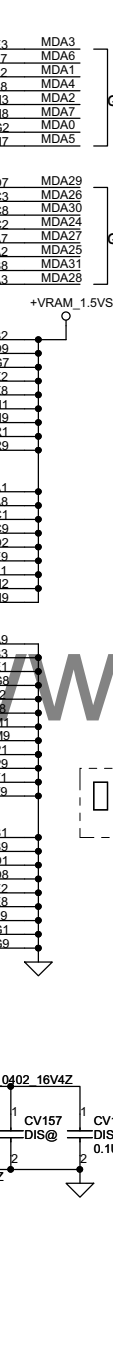
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GB2-128

Compal Electronics, Inc.			
SCHEMATIC, MB A7211			
Title			
NTN	Size	Document Number	Rev B
R&D		4019BD	
Date:	Monday, February 28, 2011	Sheet	18 of 59



<http://adf.ly/3o8pJ>

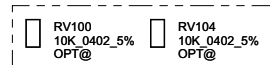
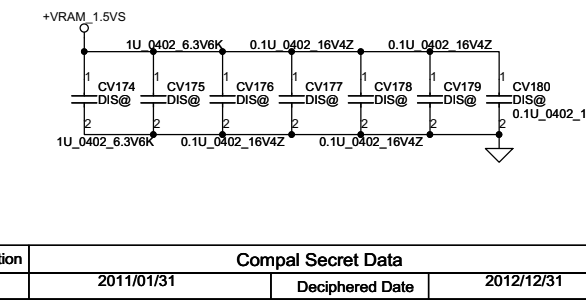
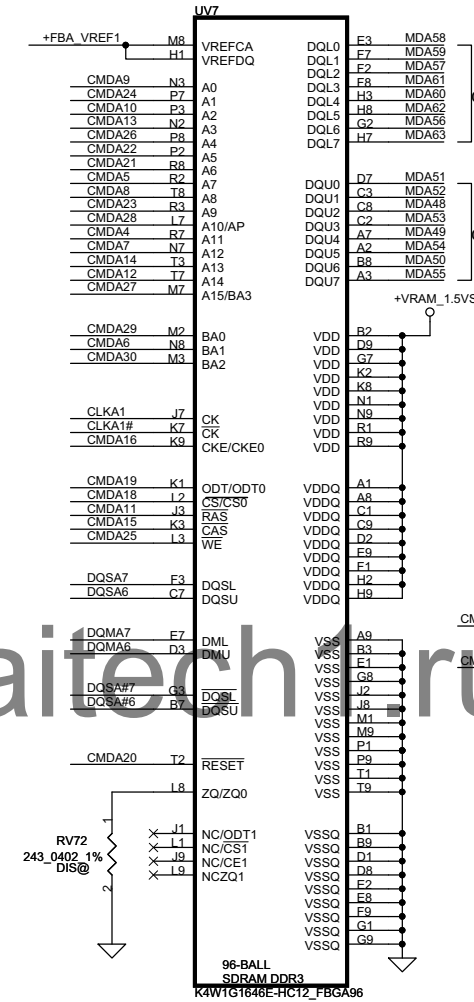
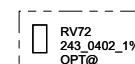
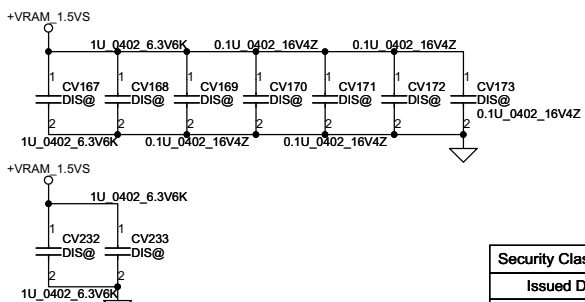
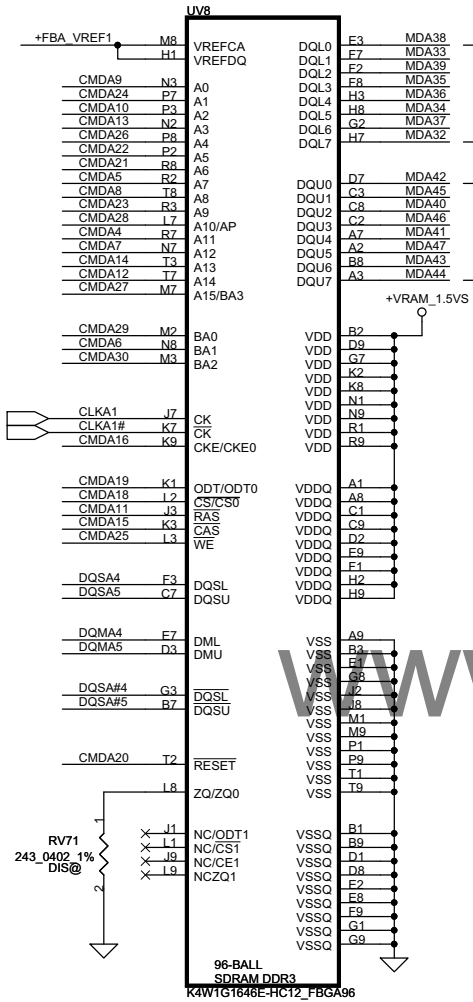
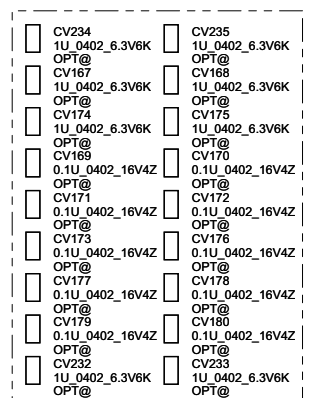
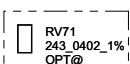
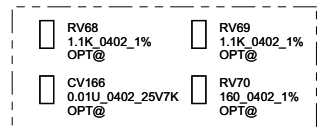
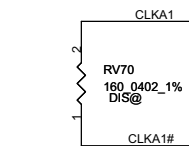
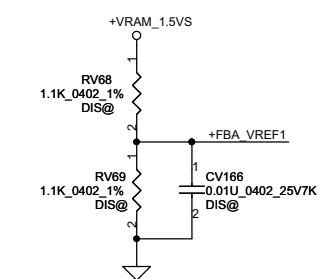


	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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Memory Partition A - Upper 32 bits

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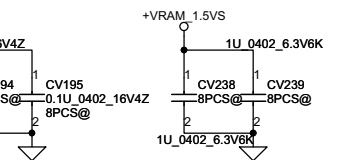
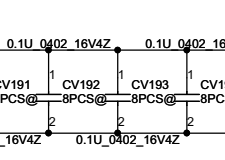
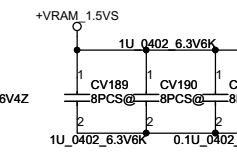
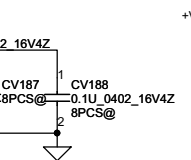


GB2-128 Mode E - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
CMD3	CKE_L
CMD8	A8
CMD2	CS0#_L
CMD21	A7
CMD24	A2
CMD23	A11
CMD26	A5
CMD7	A0
CMD15	CAS#
CMD13	BA1
CMD4	A9
CMD18	CS0#_H
CMD29	BA0
CMD27	BA2
CMD6	A3
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4
CMD12	A13
CMD28	WE#
CMD10	A1
CMD25	A10
CMD9	A12
CMD1	CS1#_L
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CMD0	ODT_L
CMD5	A6
CMD16	CKE_H
CMD20	RST
CMD14	A14
CMD30	A15

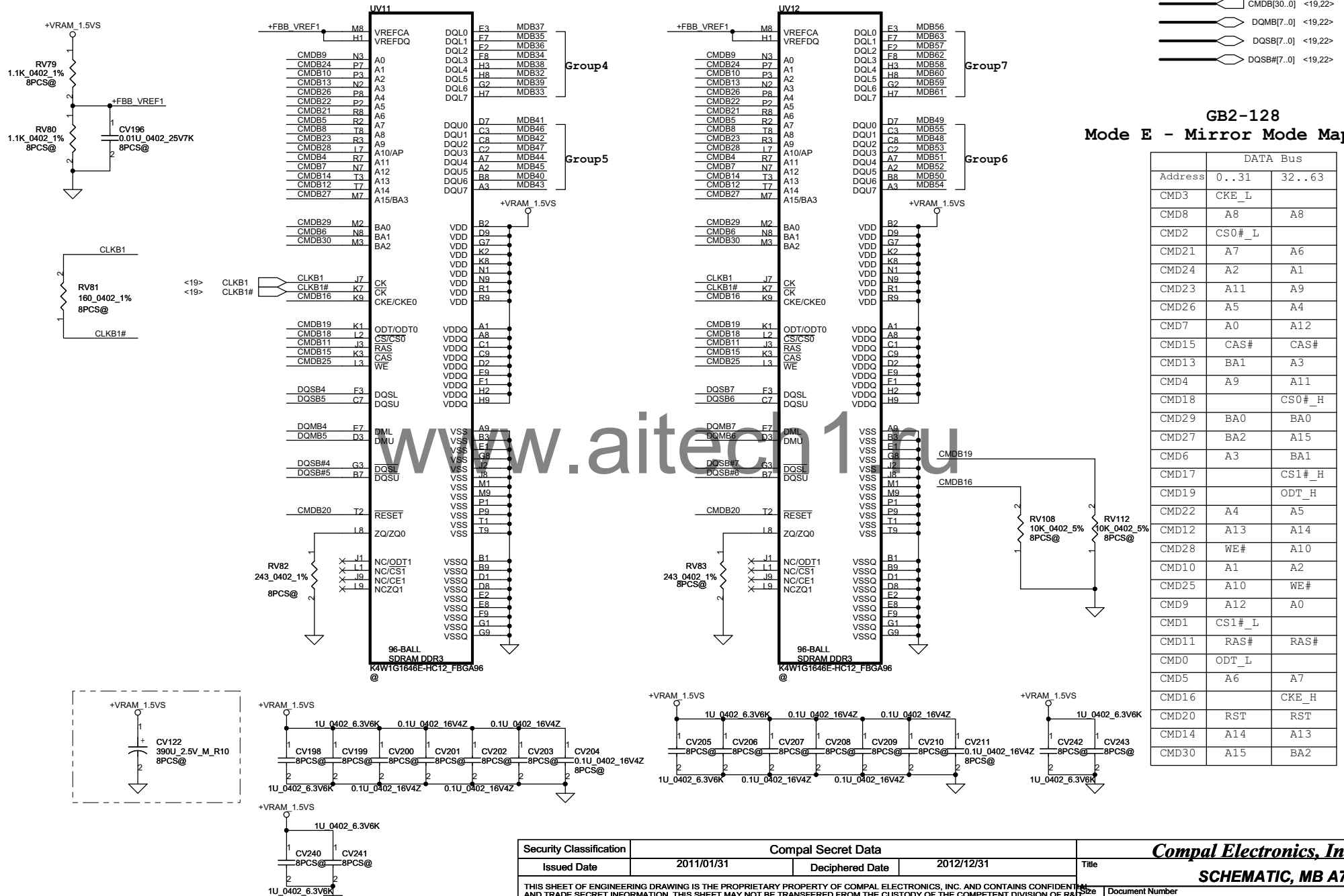
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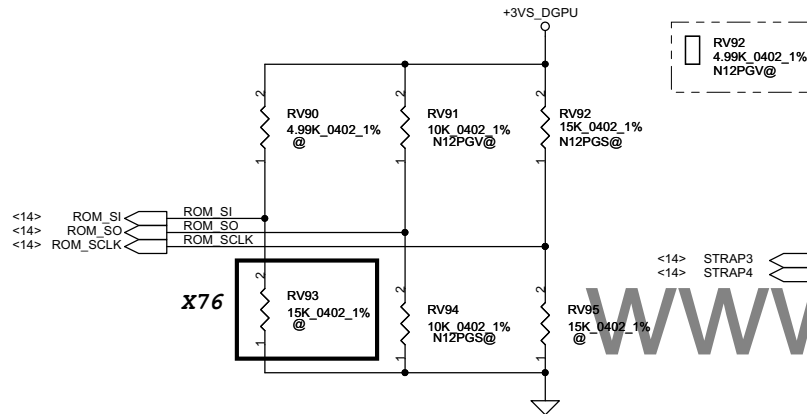
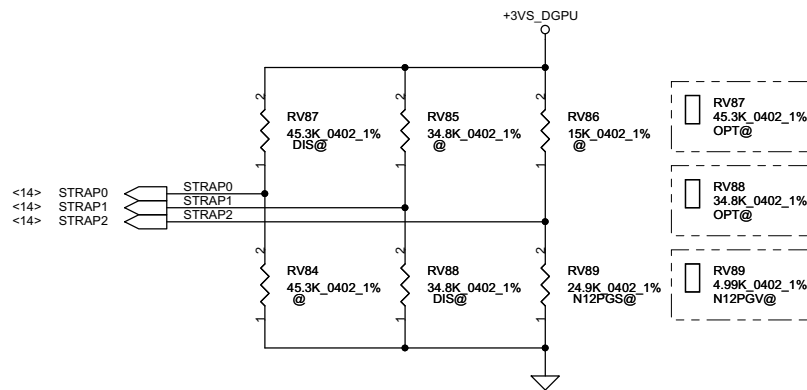


	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Memory Partition C - Upper 32 bits



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Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_DGPU	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR
ROM_SCLK	+3VS_DGPU	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG
ROM_SI	+3VS_DGPU	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]
STRAP2	+3VS_DGPU	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]
STRAP1	+3VS_DGPU	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]
STRAP0	+3VS_DGPU	USER[3]	USER[2]	USER[1]

Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GV	0x1050	Pull up 15K	Pull down 5K

GPU	DDR3 Type	VRAM	RAMCFG[3..0]	RV93
N12P-GS	64M16 900MHz	Hynix H5TQ1G63DFR-11C	512MB	0010
		SA000041S20	1GB	0010
		Samsung K4W1G1646E-HC11	512MB	0011
		SA000041T00	1GB	0011
	128M16 900MHz	Hynix H5TQ2G63BFR-11C	1GB	0110
		SA00003YO00	2GB	0110
		Samsung K4W2G1646C-HC11	1GB	0111
		SA000047Q00	2GB	0111
N12P-GV	64M16 800MHz	Hynix H5TQ1G63DFR-12C	512MB	0010
		SA0000324C0	512MB	0011
		Samsung K4W1G1646G-BC12	512MB	0011
		SA00004HS00	512MB	0011
	128M16 800MHz	Hynix H5TQ2G63BFR-12C	1GB	0110
		SA00003VS00	1GB	0111

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

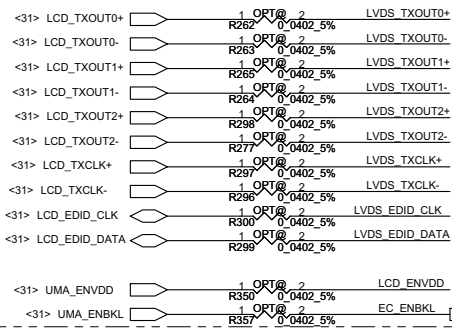
SLOT_CLOCK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

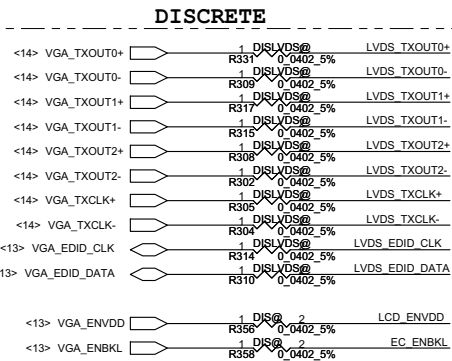
VGA_DEVICE	
0	3D Device
1	VGA Device (Default)

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OPTIMUS

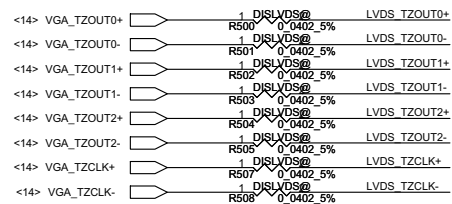


Close to LVDS Connector



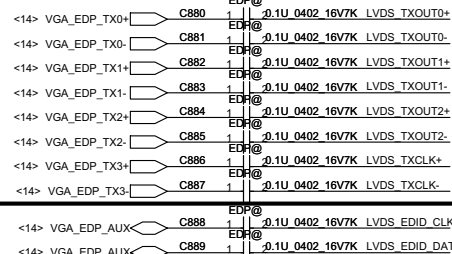
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DISCRETE for Dual Chanel Panel



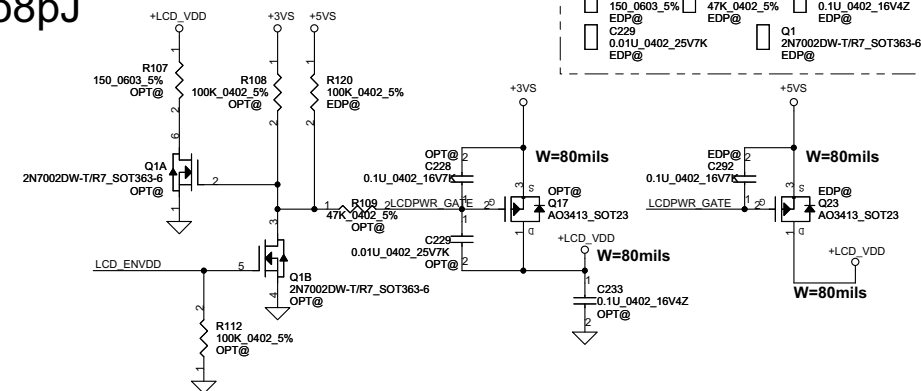
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DISCRETE for Full-HD and 3D eDP Panel

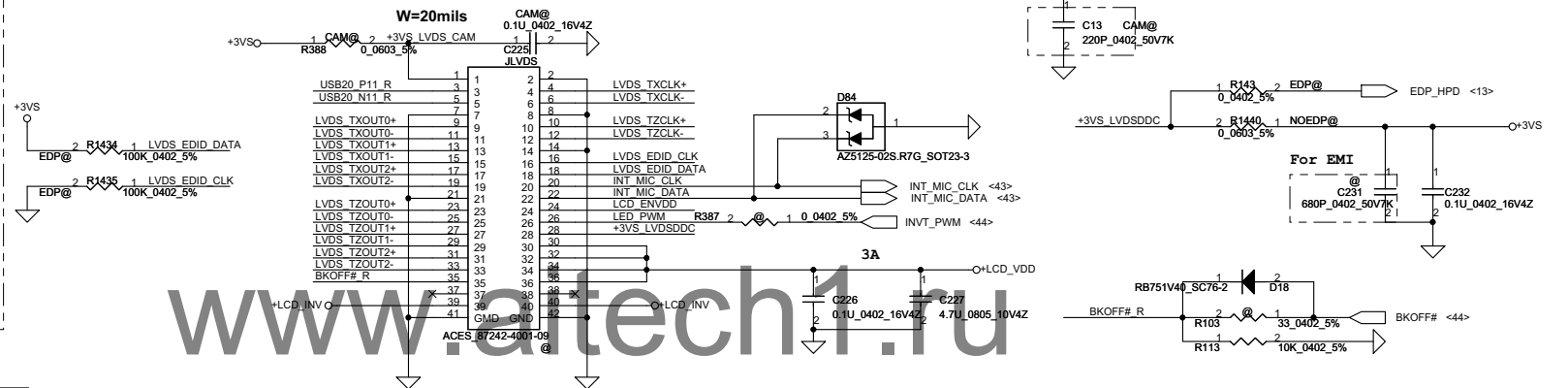


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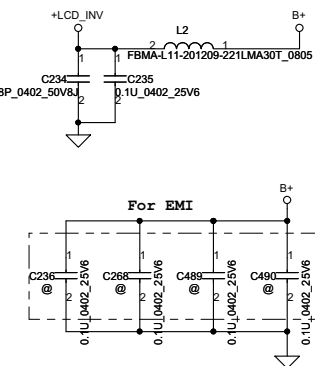
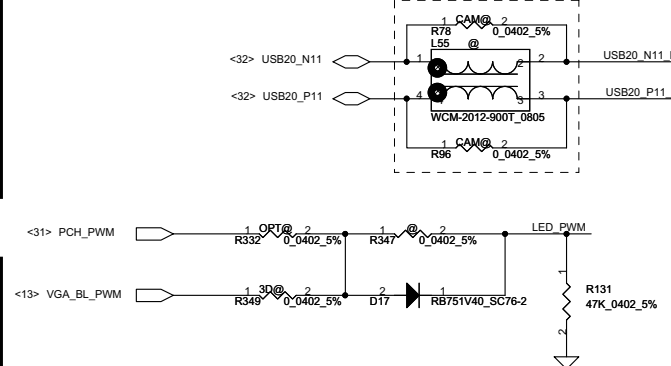
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LCD/PANEL BD. Conn.



Reserve for EMI request



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OPTIMUS

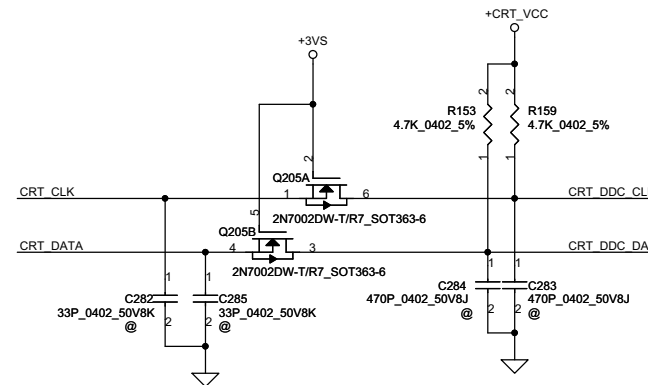
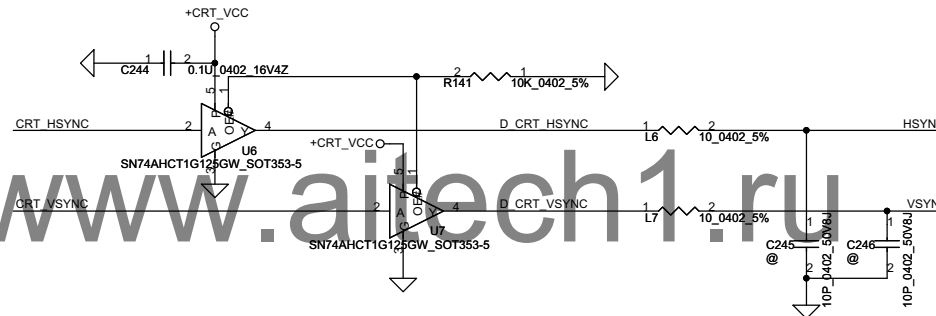
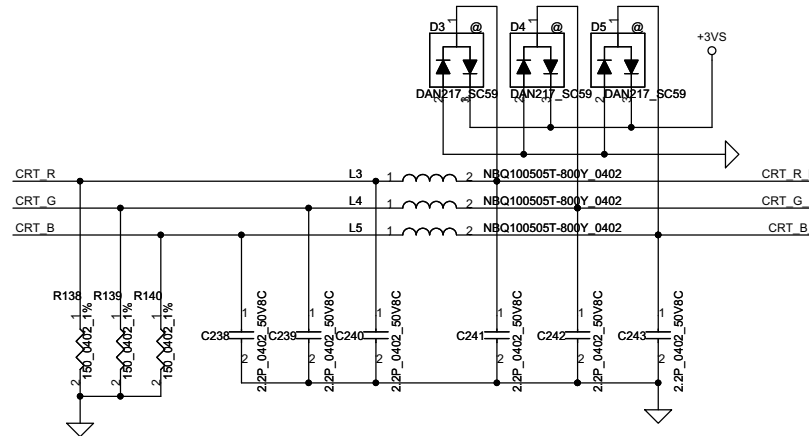
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<31> UMA_CRT_HSYNC	1 OPT@ 2	CRT_HSYNC
<31> UMA_CRT_VSYNC	1 OPT@ 2	CRT_VSYNC
<31> UMA_CRT_CLK	1 OPT@ 2	CRT_CLK
<31> UMA_CRT_DATA	1 OPT@ 2	CRT_DATA

Close to CRT Connector

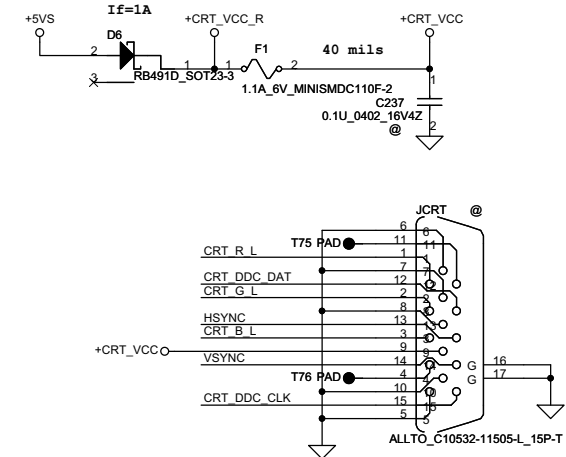
DISCRETE

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<13> VGA_CRT_G	1 DIS@ 2	CRT_G
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<13> VGA_CRT_HSYNC	1 DIS@ 2	CRT_HSYNC
<13> VGA_CRT_VSYNC	1 DIS@ 2	CRT_VSYNC
<13> VGA_CRT_CLK	1 DIS@ 2	CRT_CLK
<13> VGA_CRT_DATA	1 DIS@ 2	CRT_DATA

Close to CRT Connector

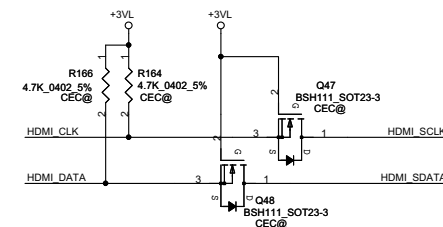
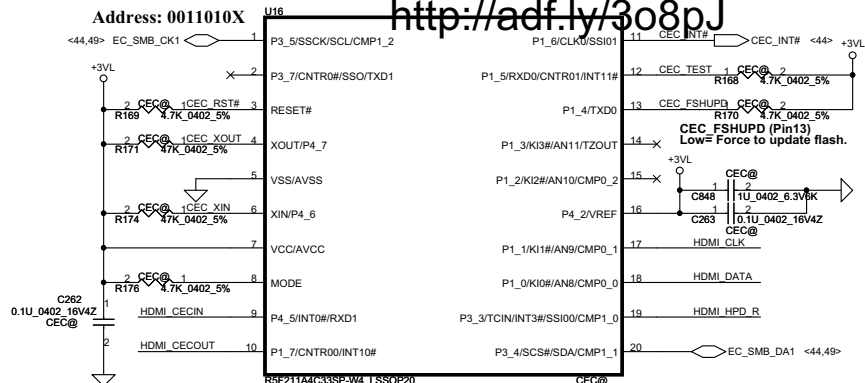
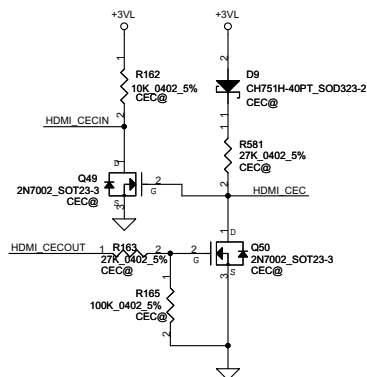


CRT CONNECTOR











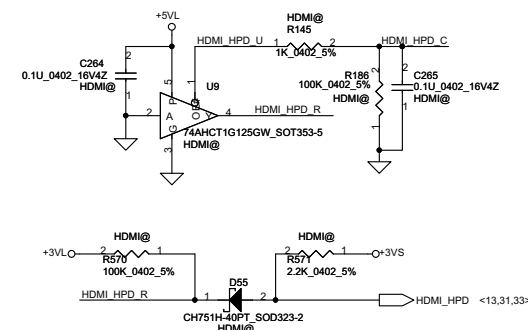
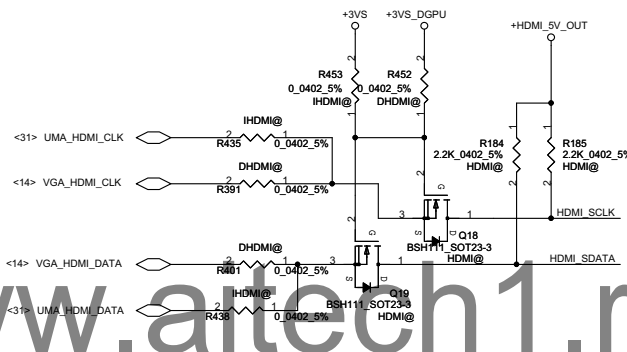
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HDMI CEC Controller



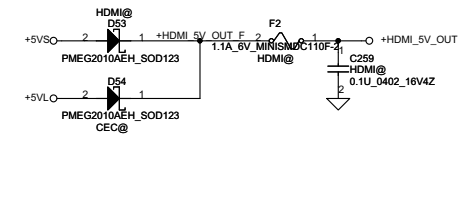
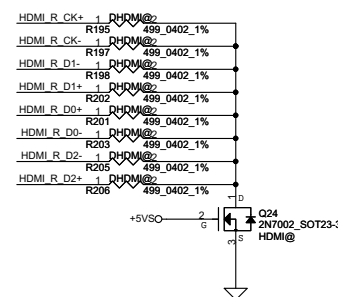
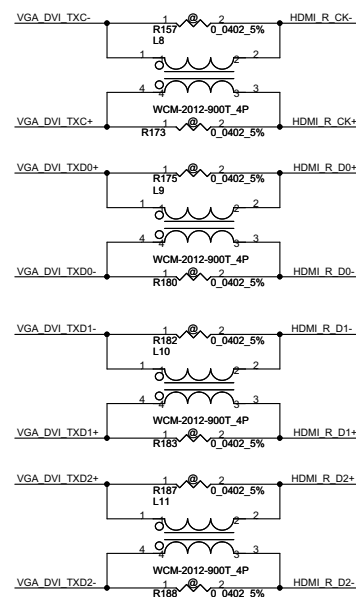
For DISCRETE

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<14> VGA_HDMI_TX0+		CV294	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0+
<14> VGA_HDMI_TX0-		CV297	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD0-
<14> VGA_HDMI_TX1+		CV299	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD1+
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<14> VGA_HDMI_TX2+		CV295	1	2	0.1U_0402_16V7K	DHDMI@	VGA_DVI_TXD2+
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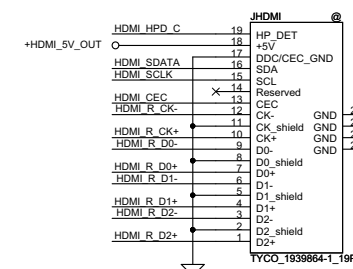


For Optimus

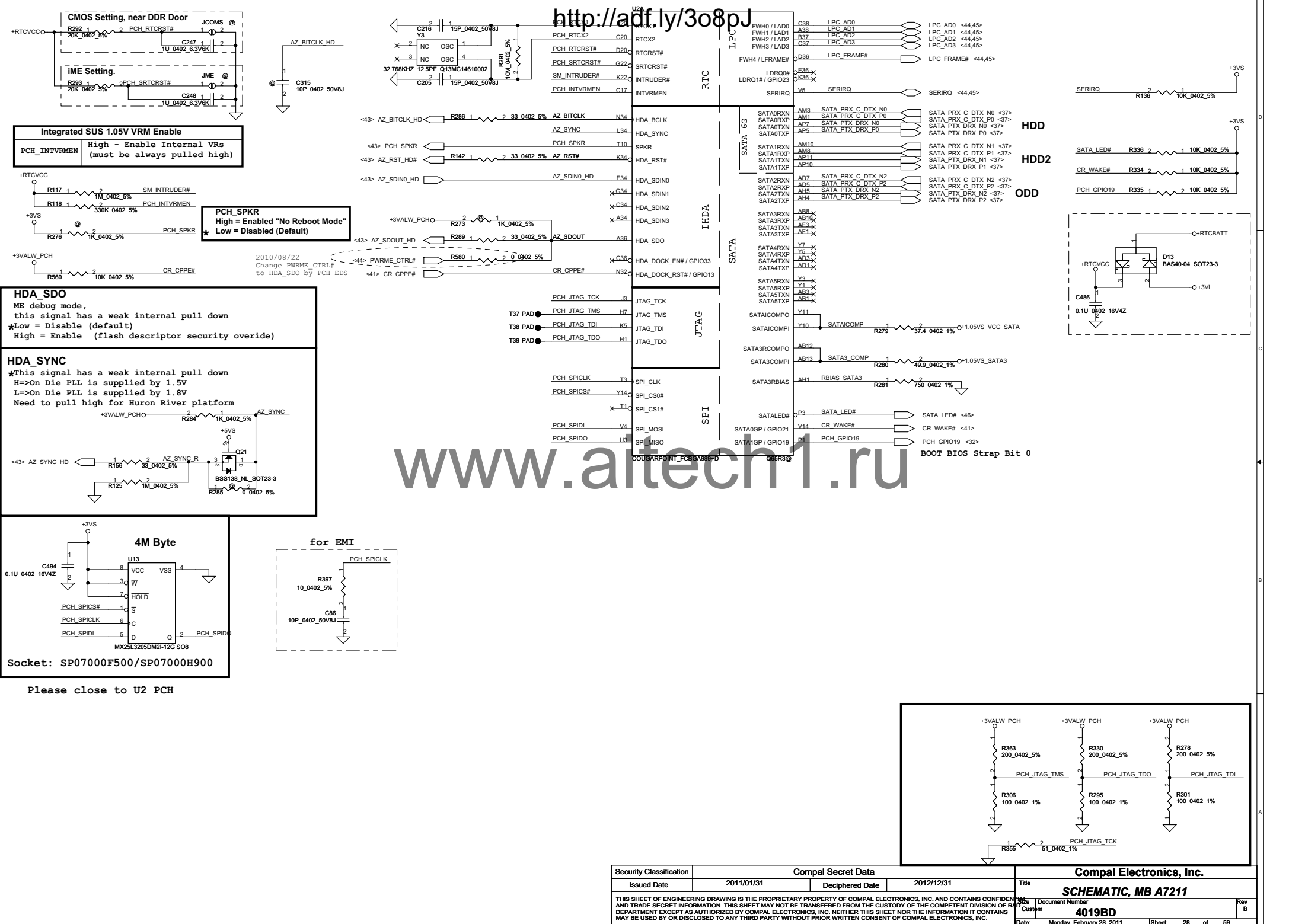
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<31>	UMA_HDMI_TX0+	CV306	1	2	0.1U_0402	16V7K	IHDM1@	VGA_DVI_TXD0+
<31>	UMA_HDMI_TX0-	CV302	1	2	0.1U_0402	16V7K	IHDM1@	VGA_DVI_TXD0-
<31>	UMA_HDMI_TX1+	CV303	1	2	0.1U_0402	16V7K	IHDM1@	VGA_DVI_TXD1+
<31>	UMA_HDMI_TX1-	CV301	1	2	0.1U_0402	16V7K	IHDM1@	VGA_DVI_TXD1-
<31>	UMA_HDMI_TX2+	CV307	1	2	0.1U_0402	16V7K	IHDM1@	VGA_DVI_TXD2+
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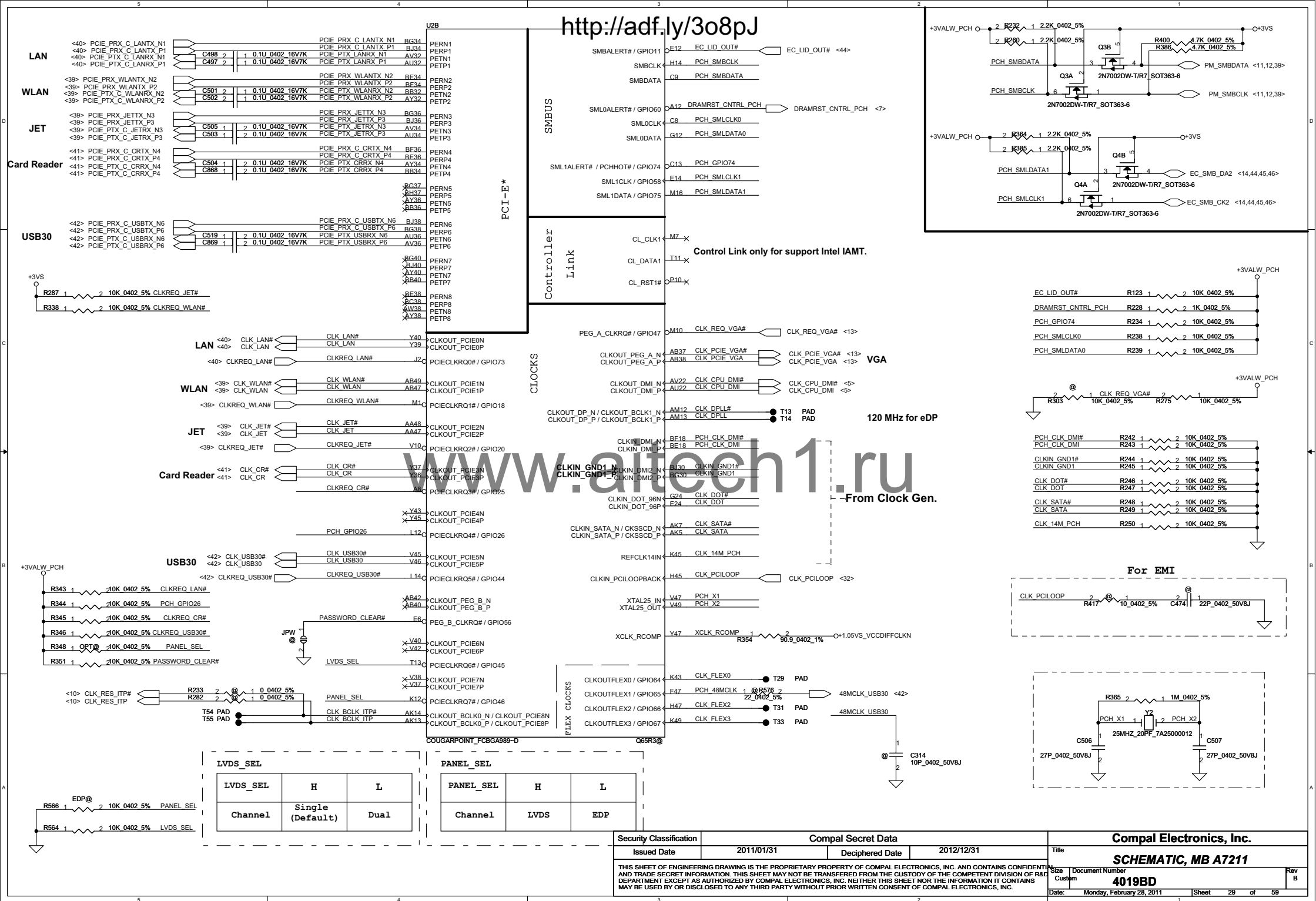


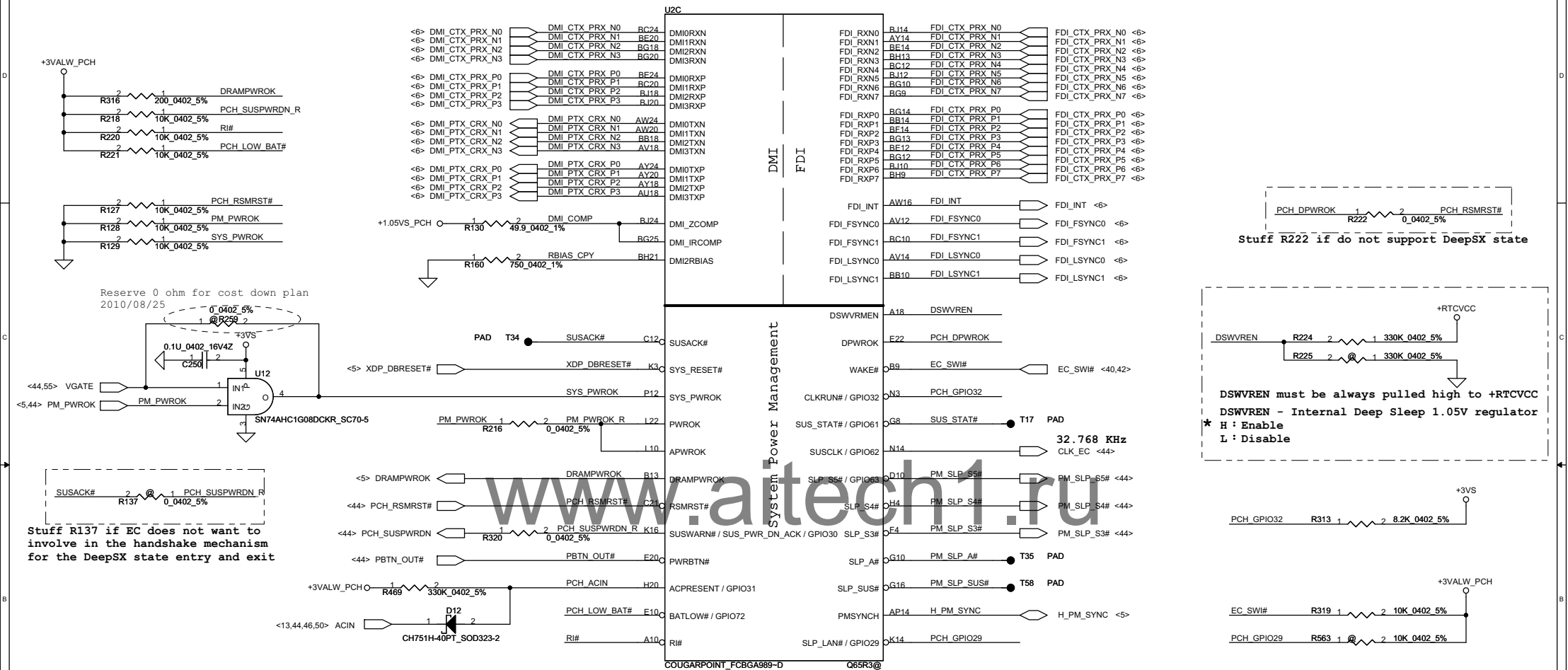
HDMI Connector

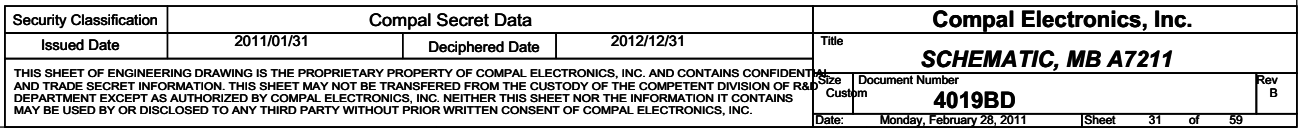


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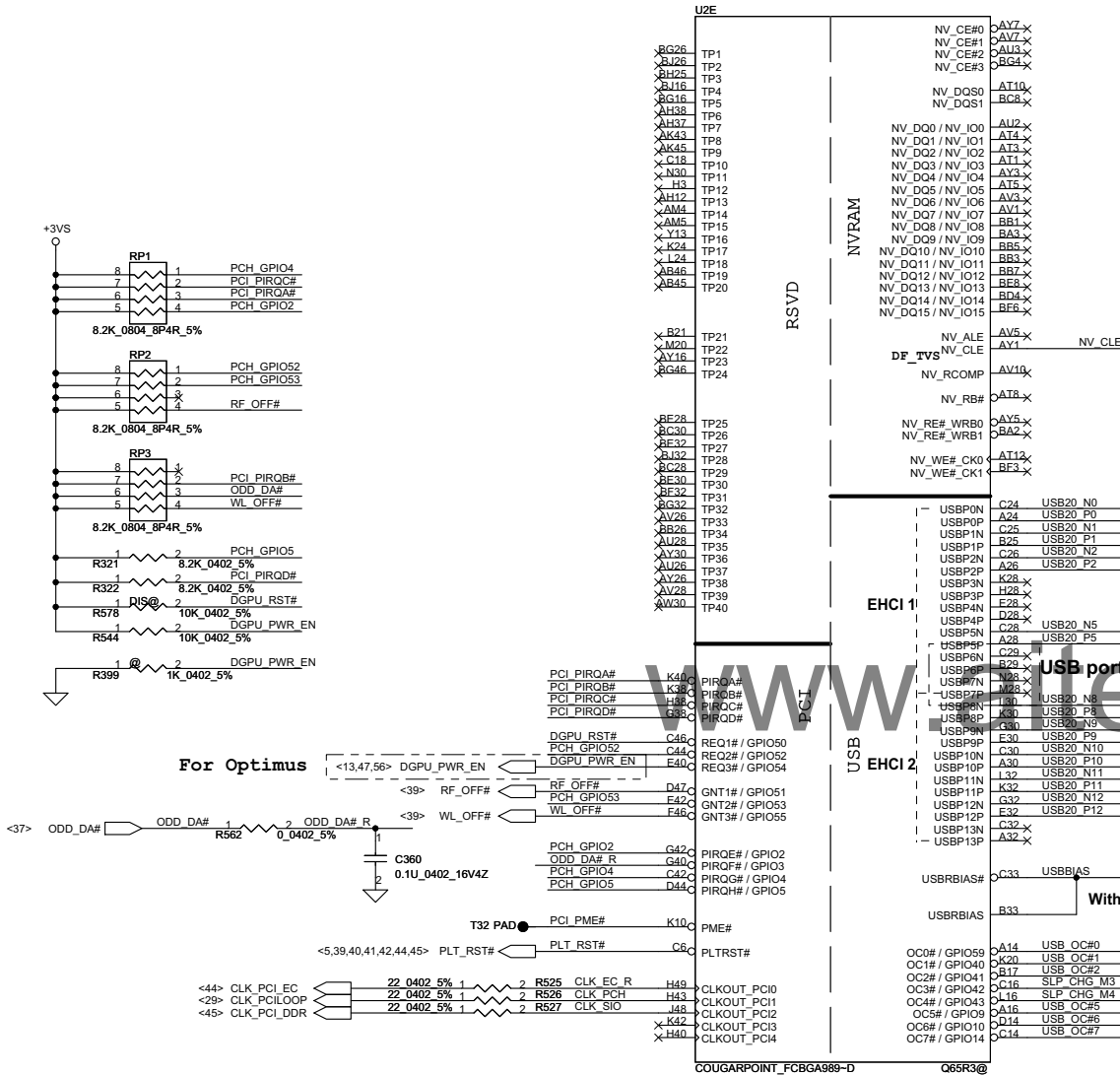
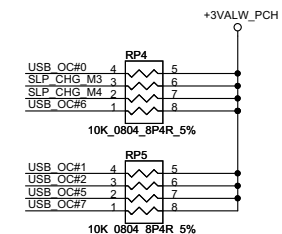
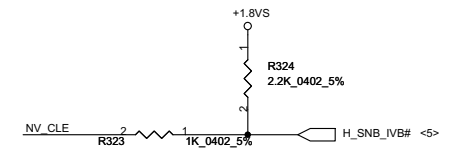






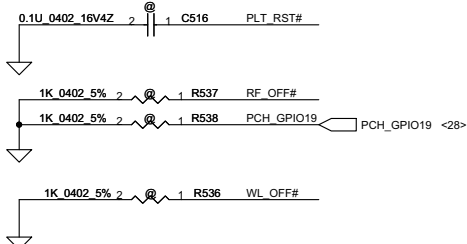


DMI & FDI Termination Voltage	
NV_CLE	Set to VCC when HIGH
	Set to VSS when LOW

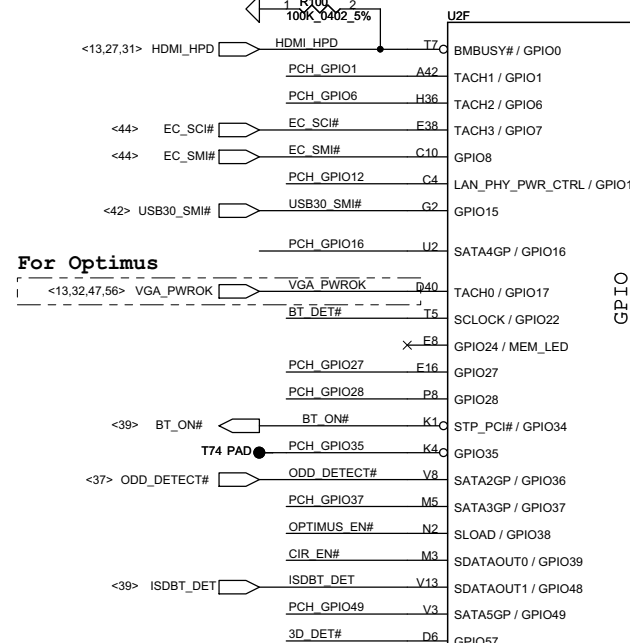
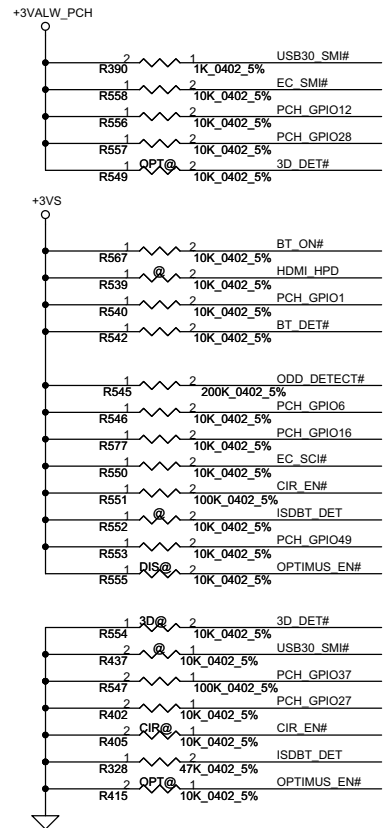


Boot BIOS Strap		
RF_OFF#	PCH_GPIO19	Boot BIOS Loaction
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI *

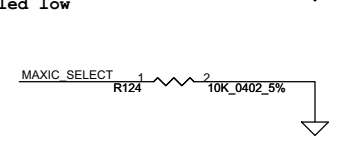
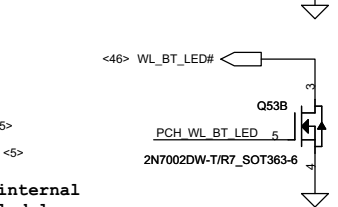
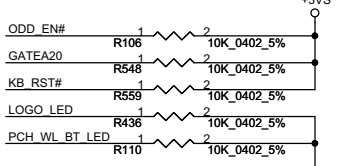
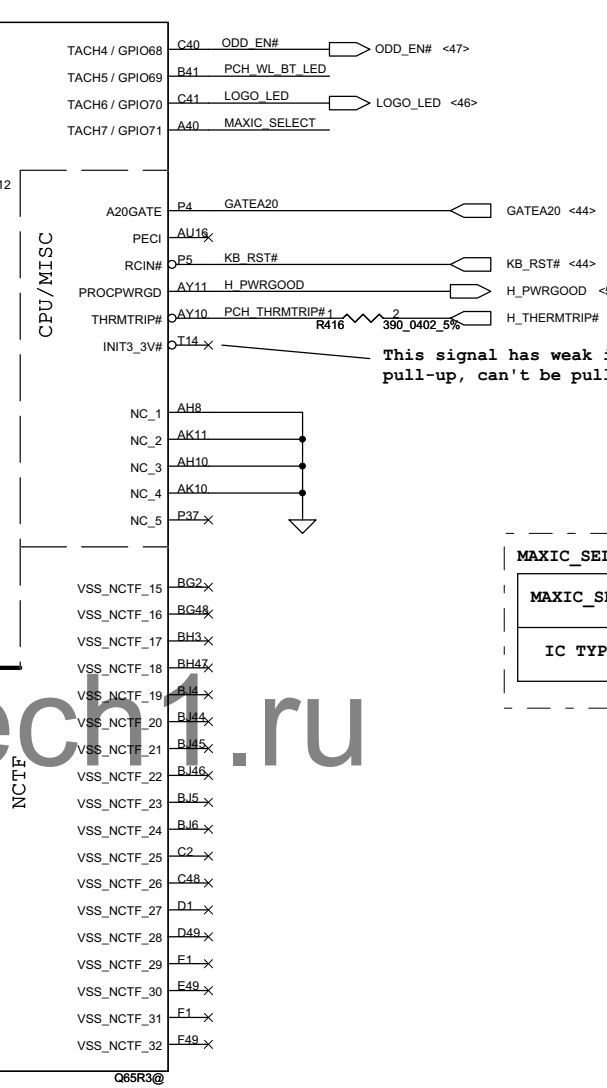
A16 Swap Override Strap	
WL_OFF#	★ Low= A16 swap override Enable High= A16 swap override Disable



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For Optimus



MAXIC_SELECT		
MAXIC_SELECT	H	L
IC TYPE	MAX14550E	MAX14566B

GPIO28

On-Die PLL Voltage Regulator

H: Enable

L: Disable

R325 1 2 1K 0402 5% PCH_GPIO28

3D_DET#	H	L
SKU	OPT	3D

GPIO8

Integrated Clock Chip Enable (Removed)

H: Disable

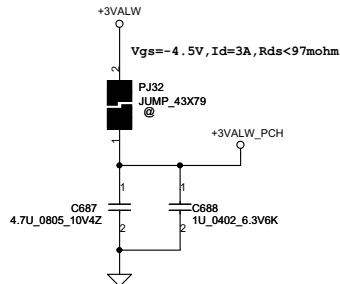
L: Enable

R326 1 2 1K 0402 5% EC_SMI#

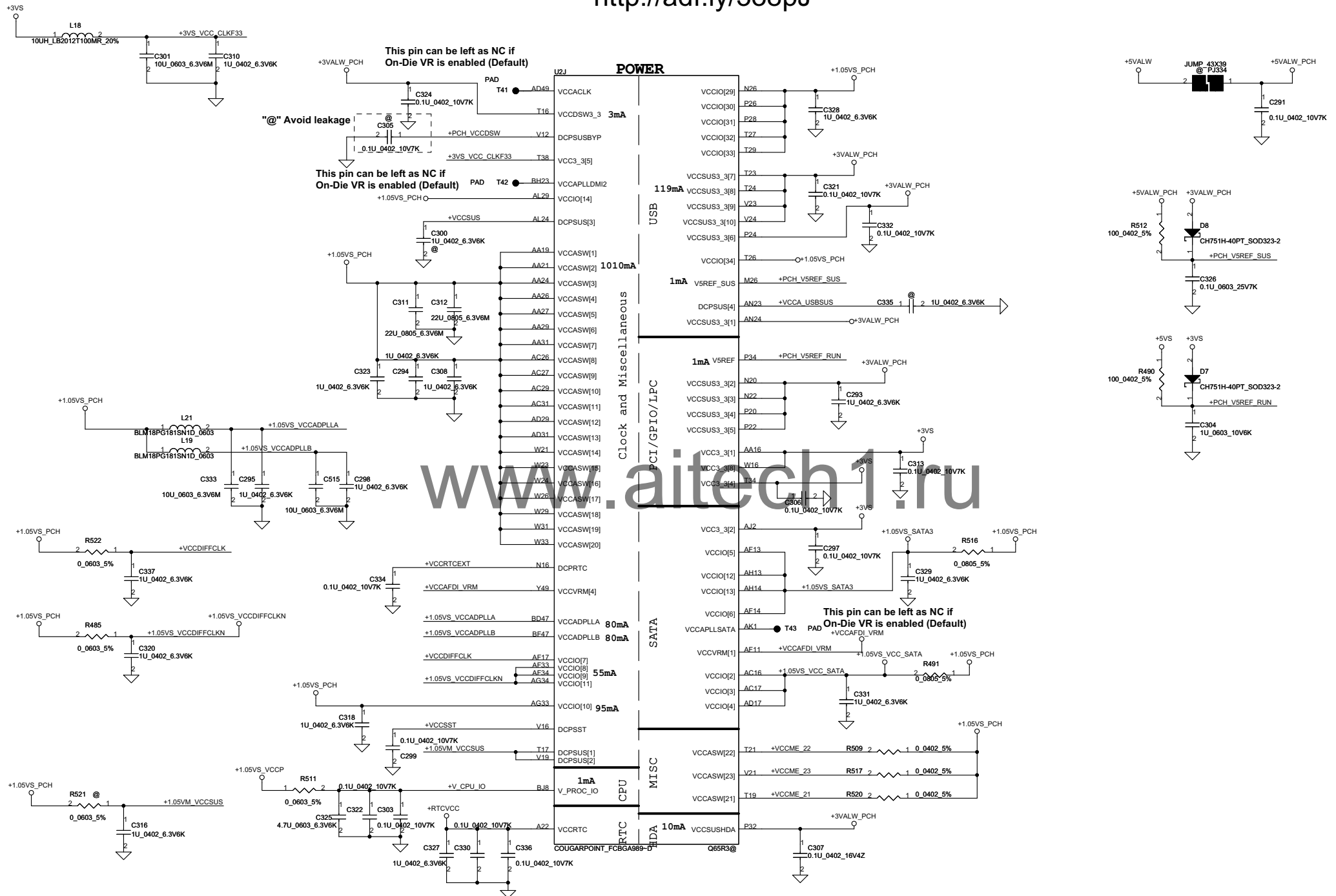
Integrated clock enable functionality is achieved by soft-strap

The current default is clock enable

OPTIMUS_EN#	H	L
SKU	Discrete	Optimus

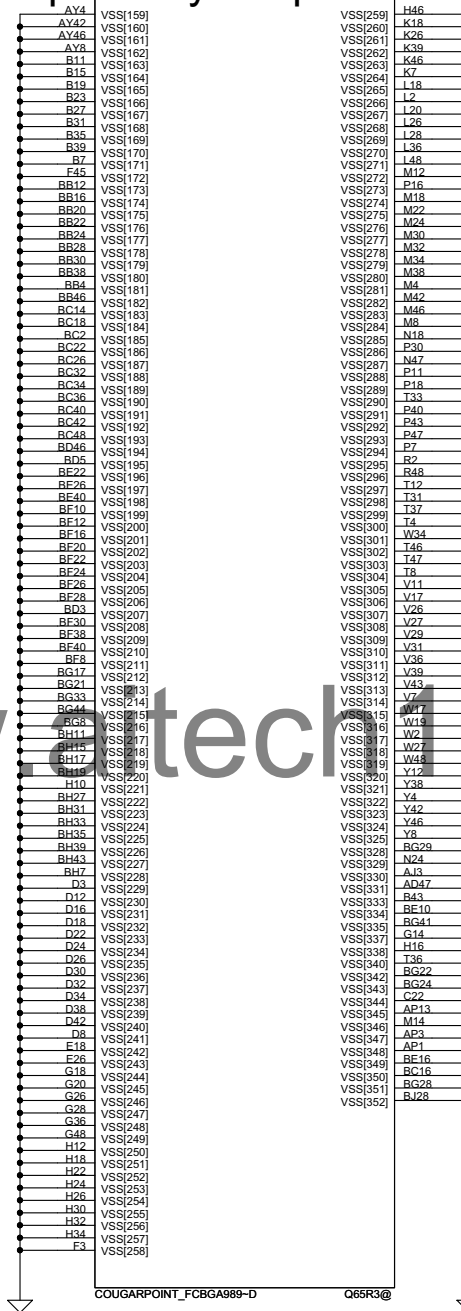
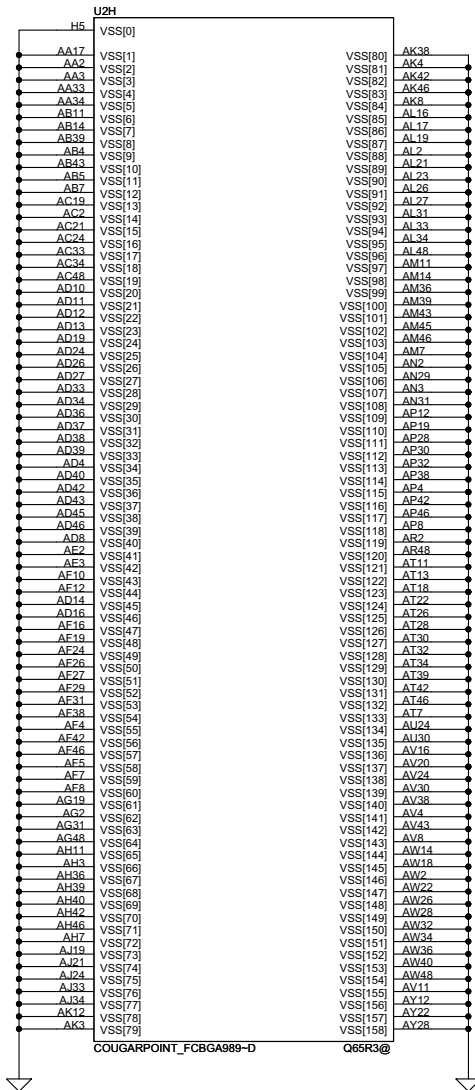


PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADFLLA	1.05	0.08
VCCADPLLB	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTERM	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSusHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCITX LVDS	1.8	0.06



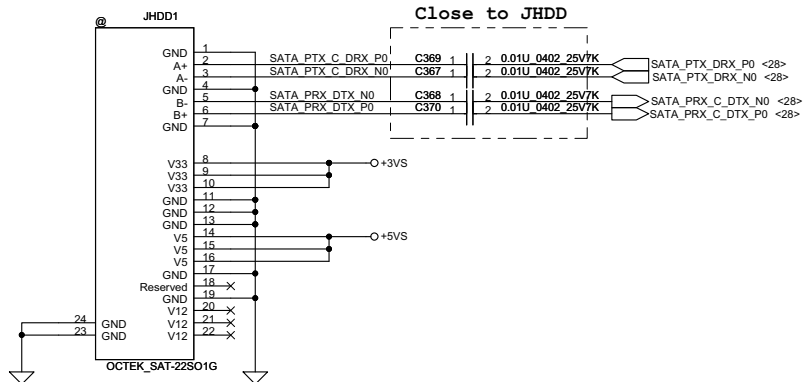
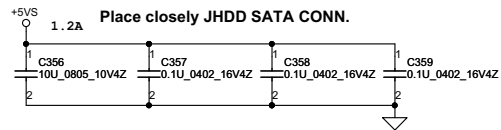
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http://adf.ly/3o8pJ

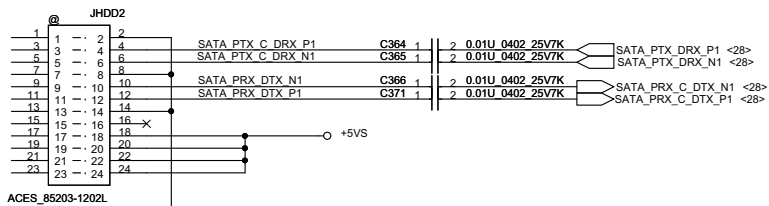
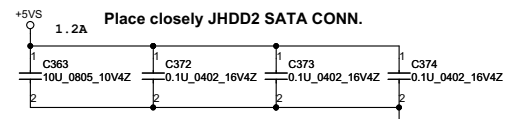


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SATA HDD
Conn. +5

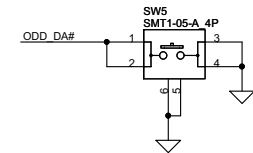
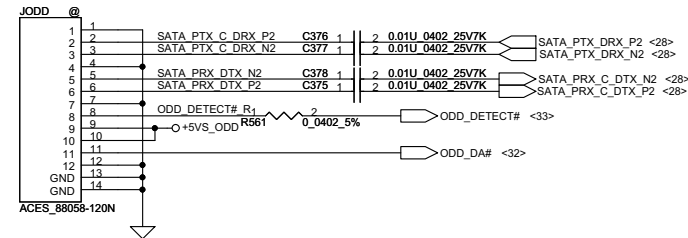


SATA 2nd HDD Conn.

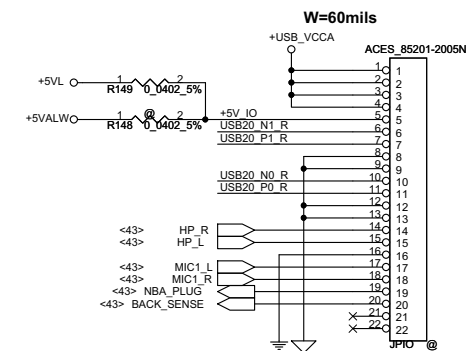
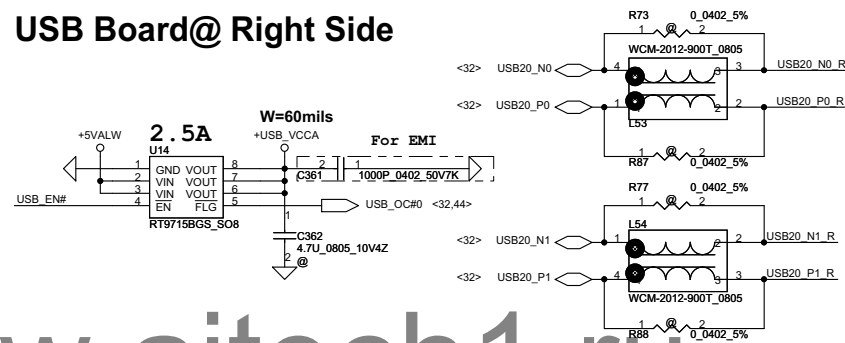


Confirm SSD need 3V or not.

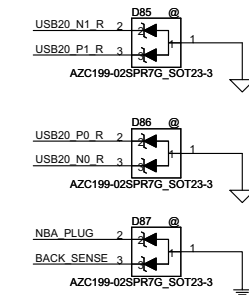
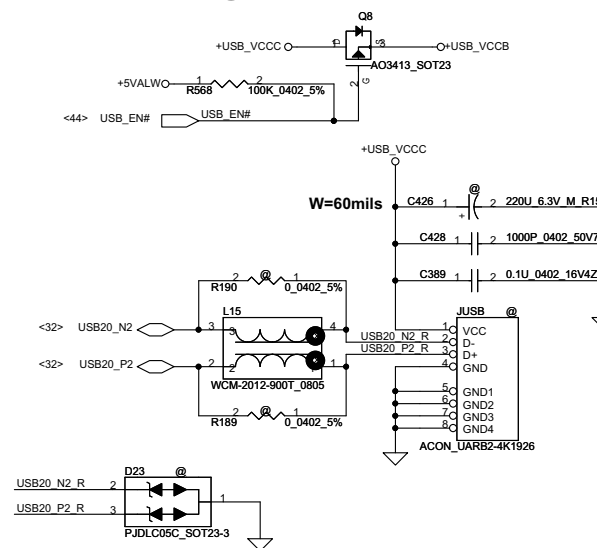
SATA on Dell.com <http://adf.ly/3o8pJ>



USB Board@ Right Side



USB Board@ Left Side

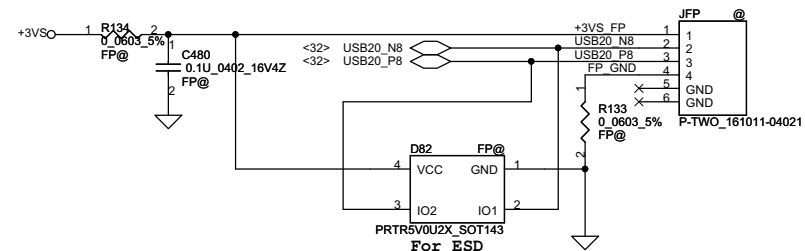


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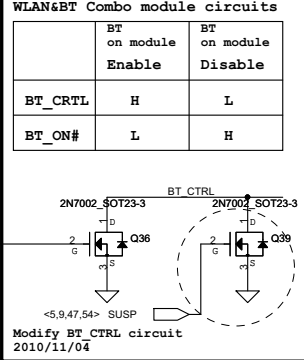
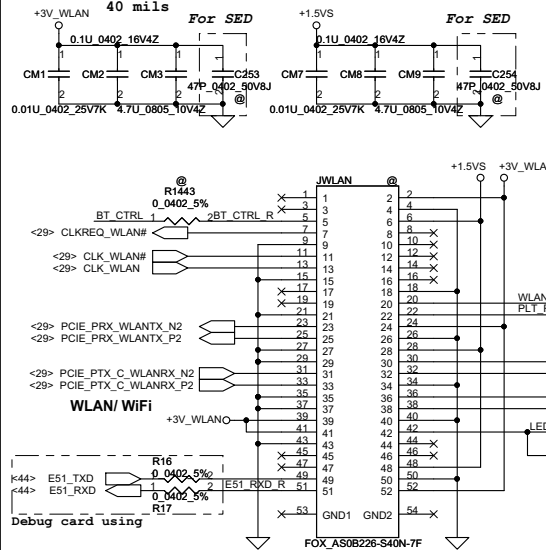
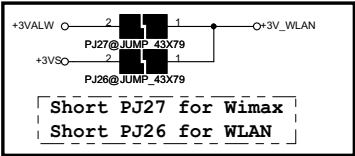


Finger printer

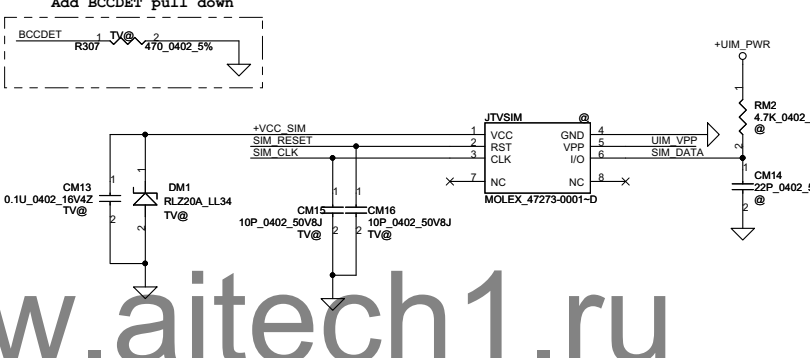
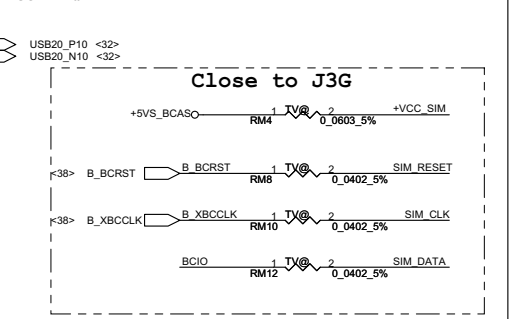
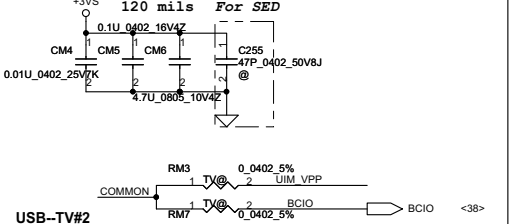
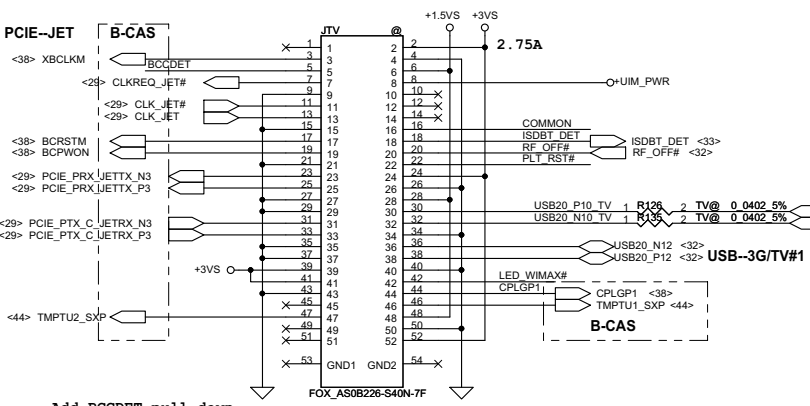


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Slot 1 Half PCIe Mini Card-WLAN/ WiMax



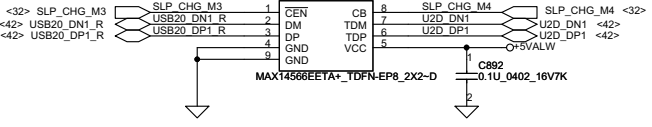
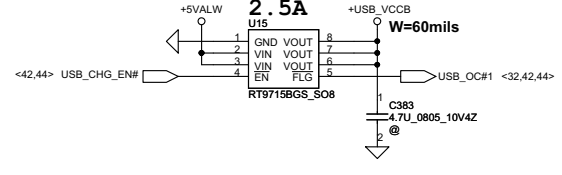
Slot 2 Full PCIe Mini Card-3G/ TV Tuner



USB Sleep & Charge Auto-Mode Mode3/Mode4

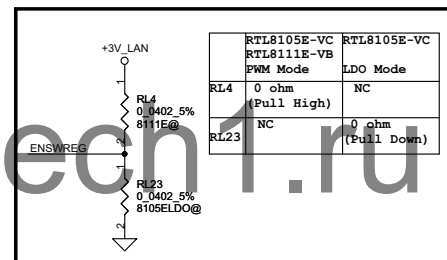
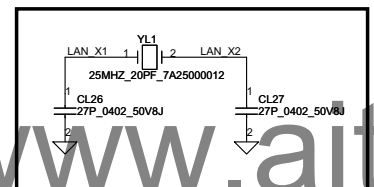
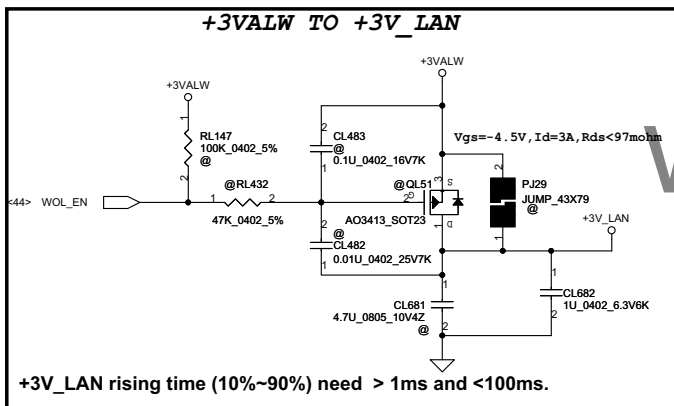
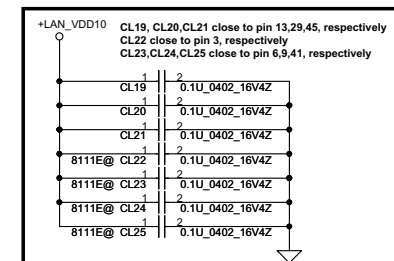
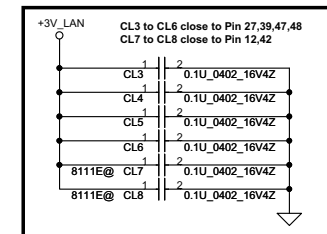
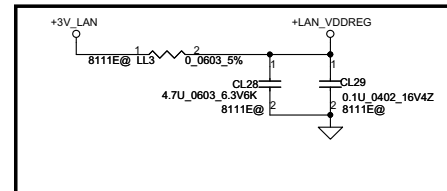
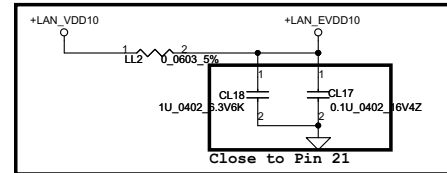
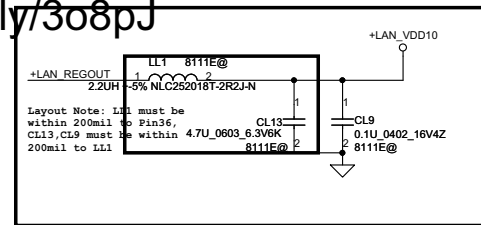
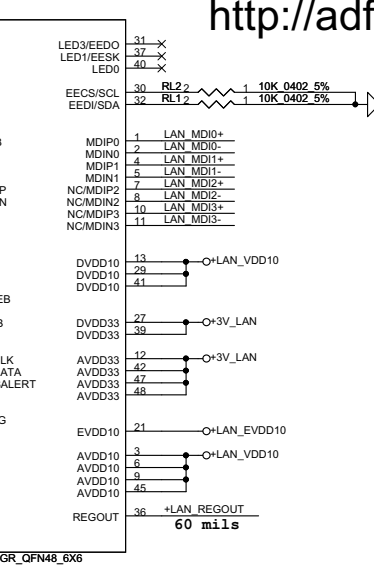
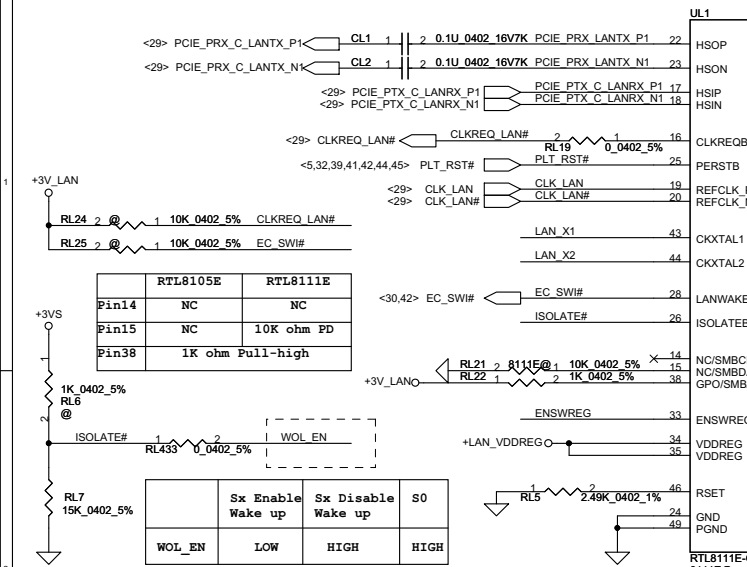
MAX14566B		
CB0 SLP_CHG_M4	CB1 (CEN#) SLP_CHG_M3	STATUS
0	0	AUTO MODE
0	1	Force Dedicated charger mode (MODE3)
1	X	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

MAX14566E	
CB0: SLP_CHG_M4	STATUS
0	AUTO MODE
1	Pass-Through (USB) Mode: Connect DP/DM to TDP/TDM

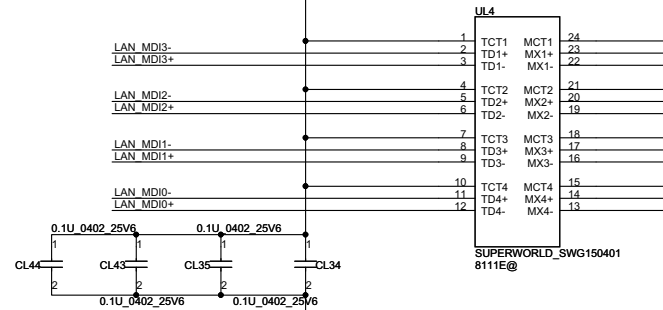
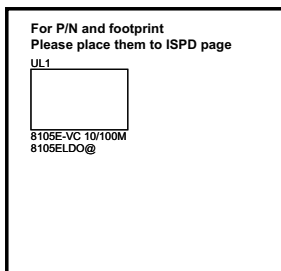
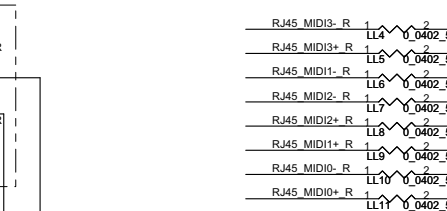
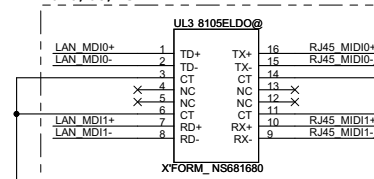


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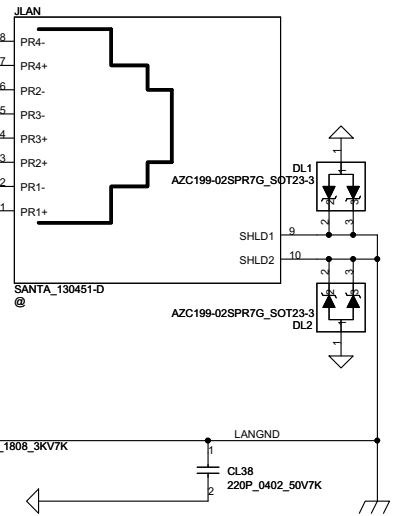


Add UL3 at DVT 2010/08/25

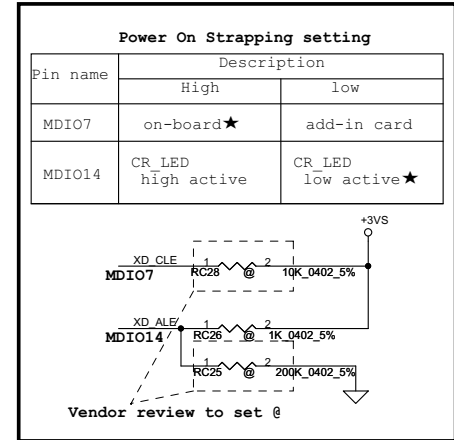
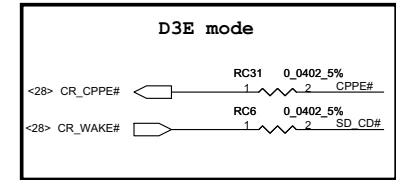
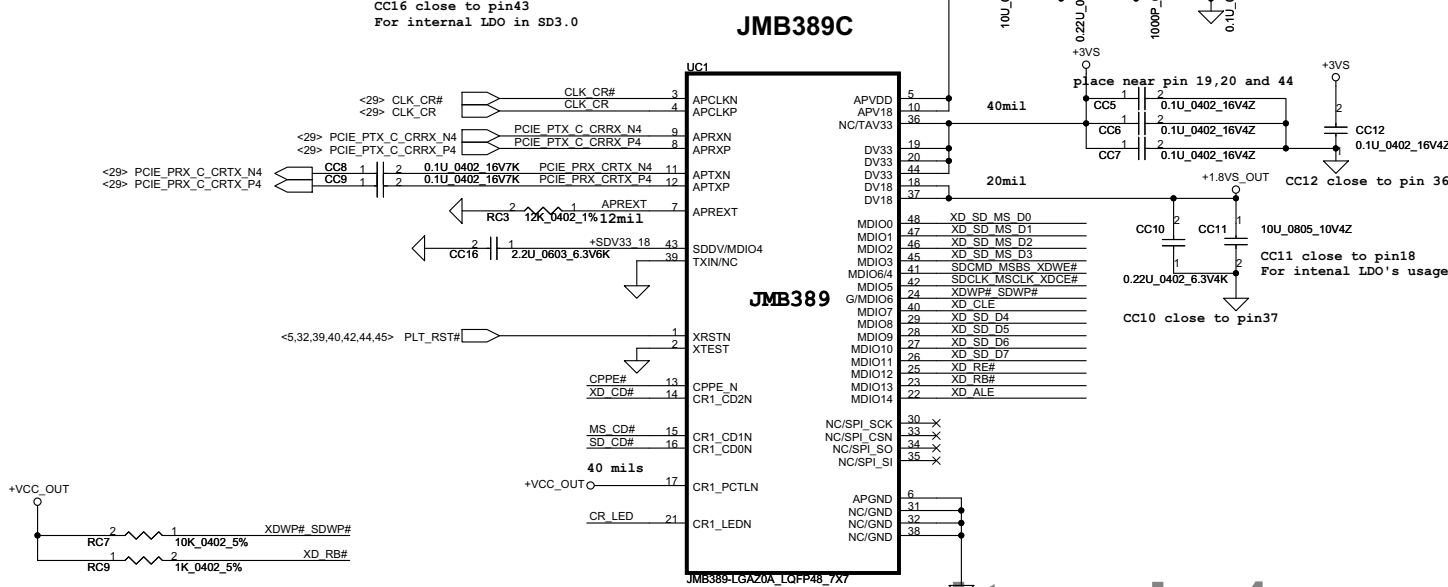


Place CL34, CL35, CL43, CL44 to colse to LAN chip

LAN Conn.

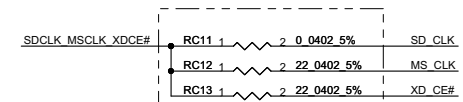
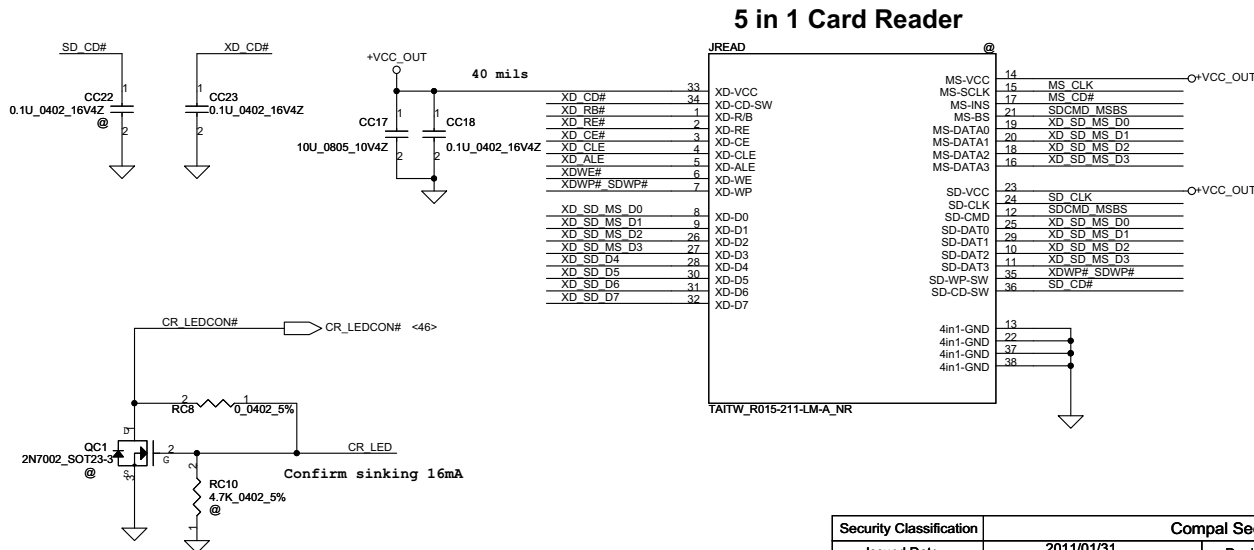
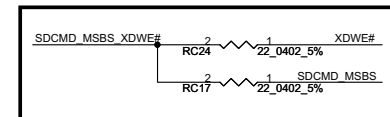


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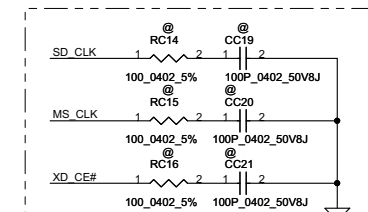


www.aitech1.ru

Add RC24 and RC17 close to UC1 for xD issue



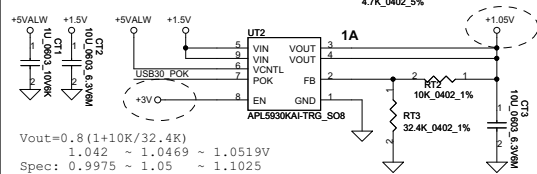
Reserved for EMI, close to UC1.42
Change RC11 from 22ohm to 0ohm
in order fix SDXC performance low.



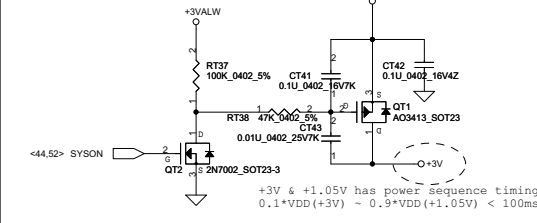
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[ _ _ _ _ _ ]
Reserved for EMI, close to JREAD
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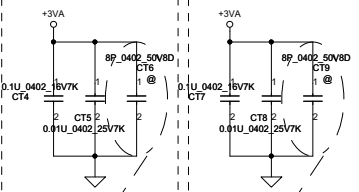
+1.5V to +1.05V Transfer



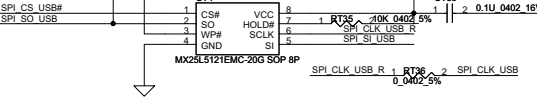
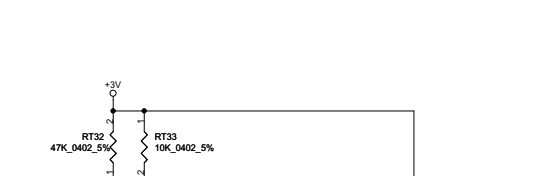
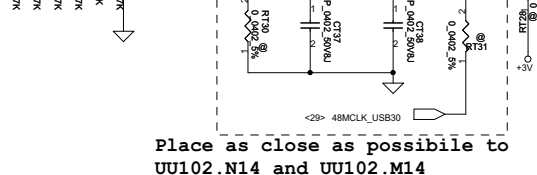
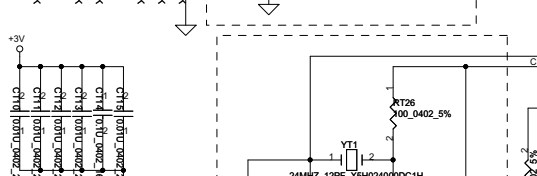
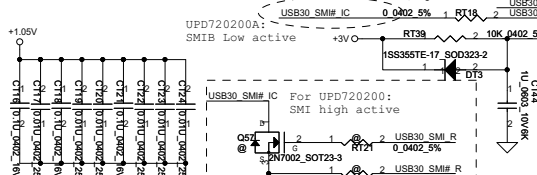
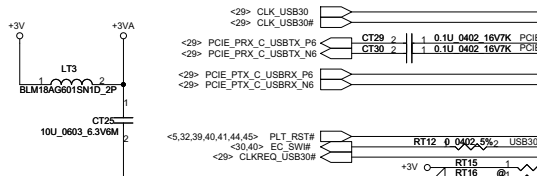
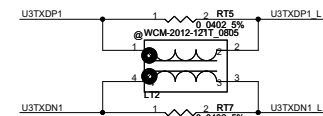
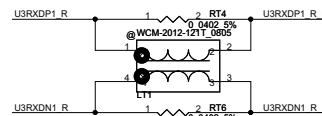
+3VALW to +3V Transfer



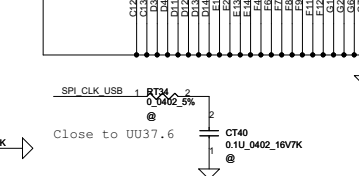
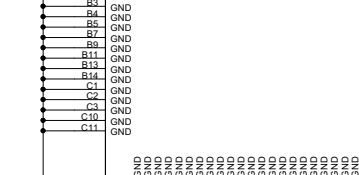
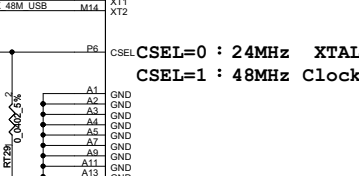
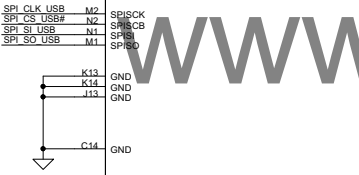
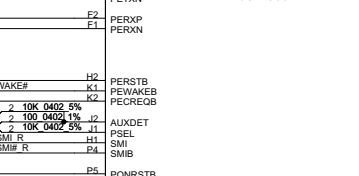
Close to U102.D7 Close to U102.P13



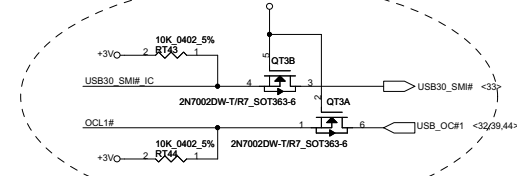
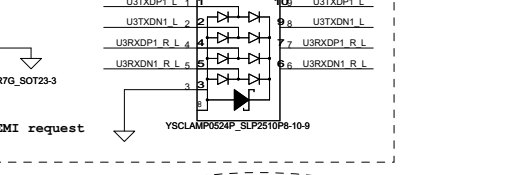
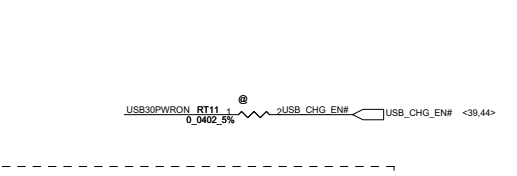
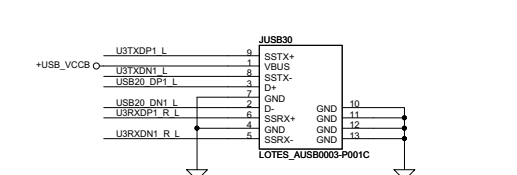
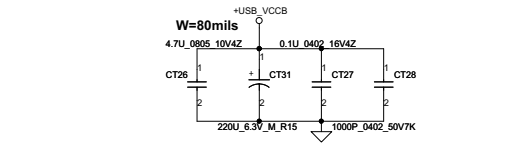
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+3V:200mA
+1.05V:800mA



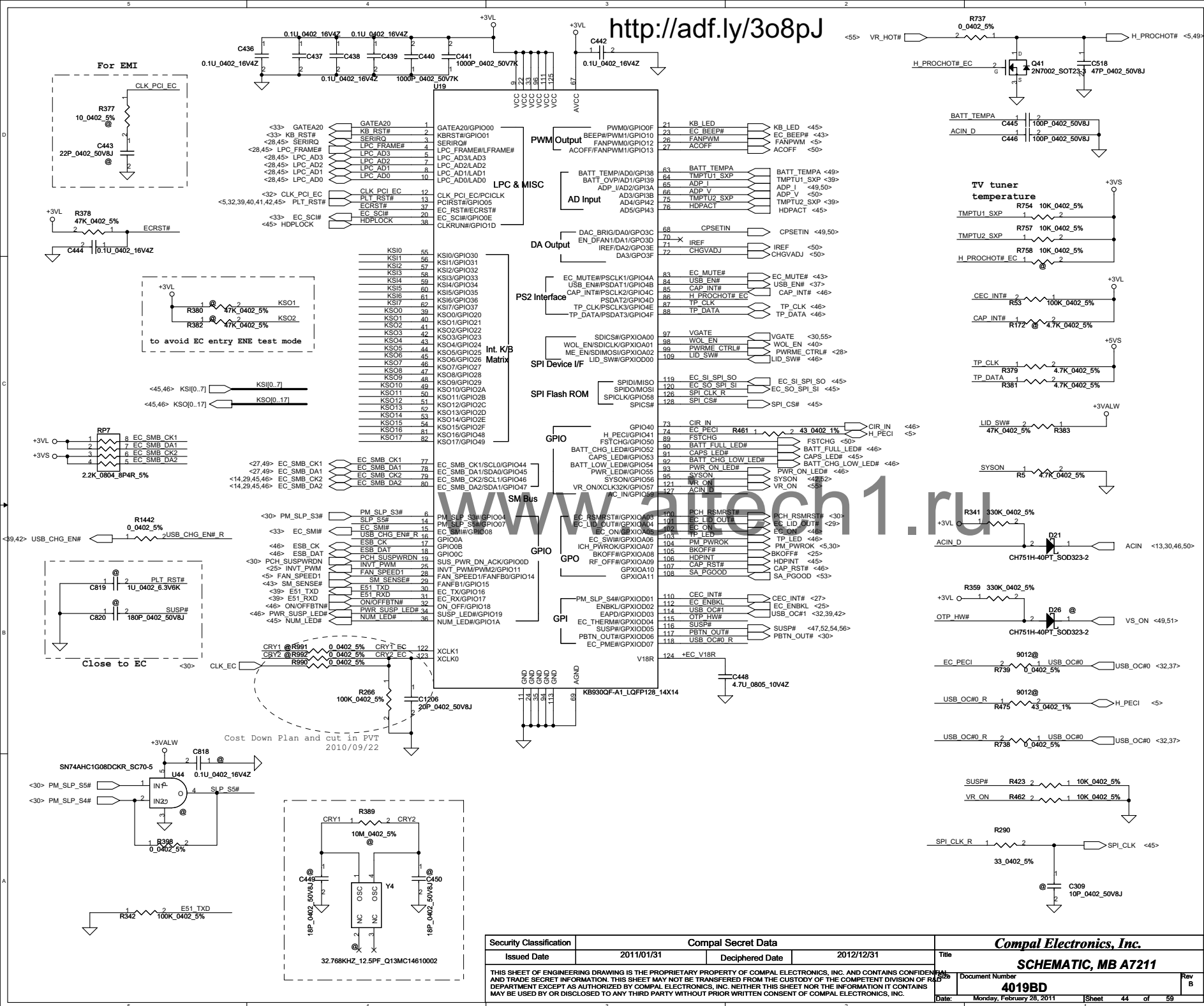
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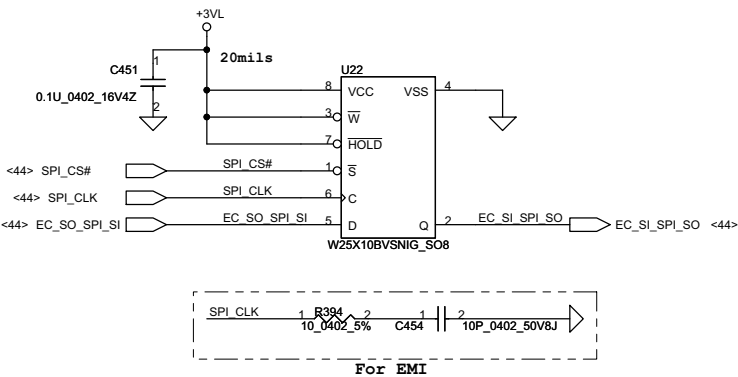
2010/09/17 Add Level shift to avoid +3V leakage from +3VALW_PCH

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2011/01/31		2012/12/31		4019BD	
2011/01/31		2012/12/31		Monday, February 28, 2011	
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http://adf.ly/3o8pJ

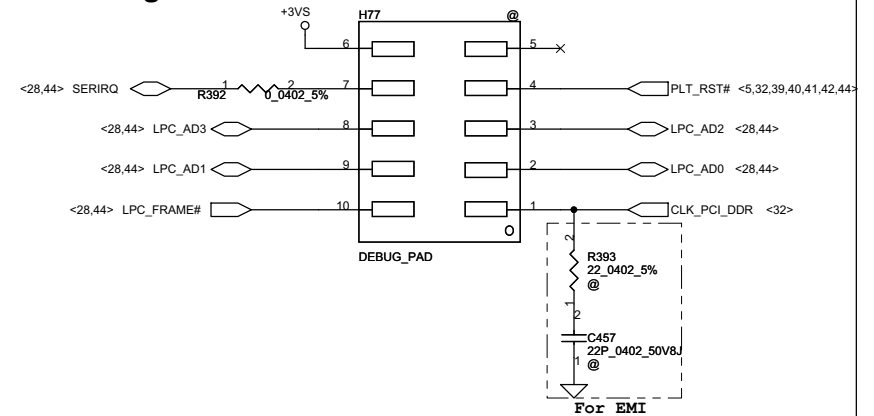


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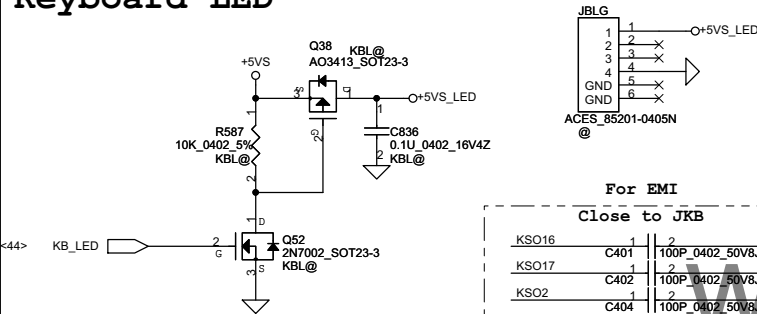


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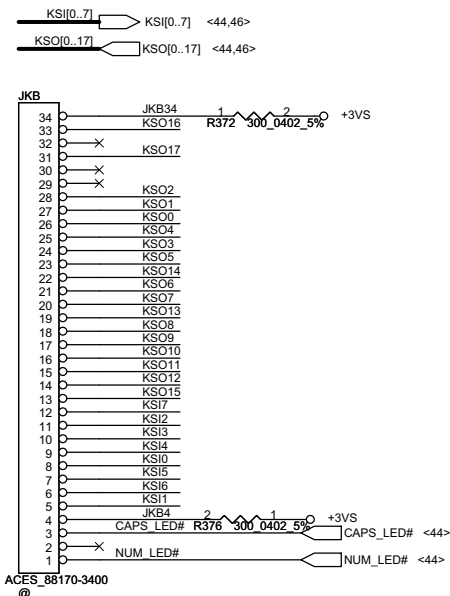
LPC Debug Port



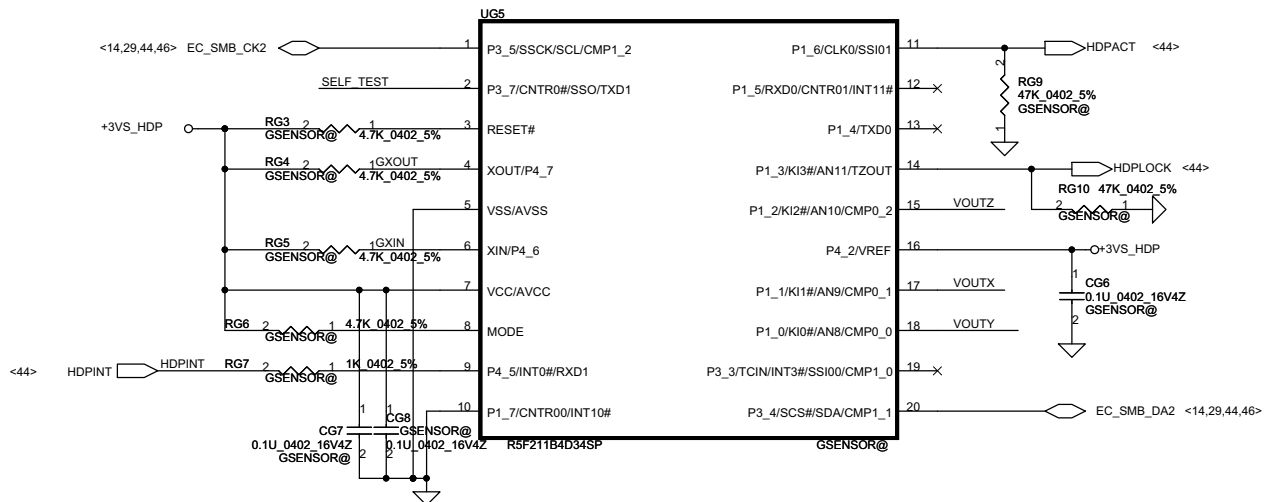
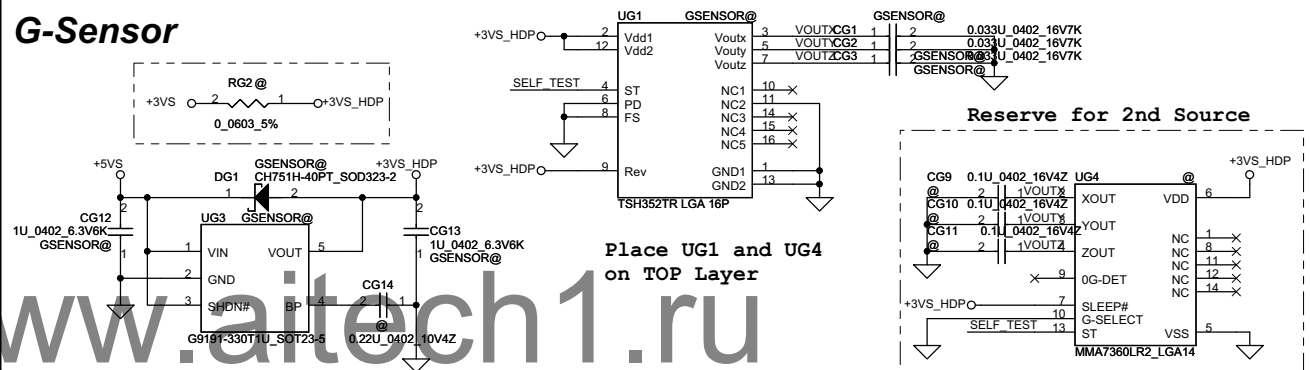
Keyboard LED



KEYBOARD CONN.

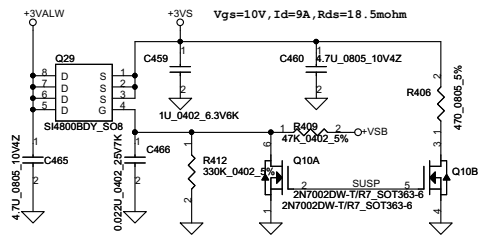


G-Sensor

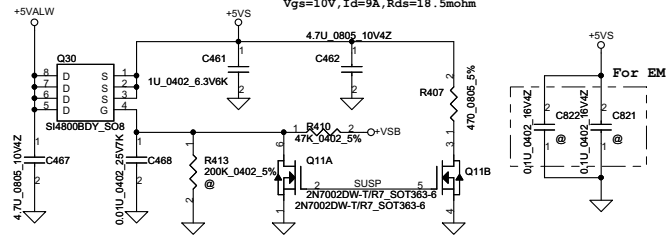


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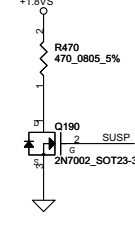
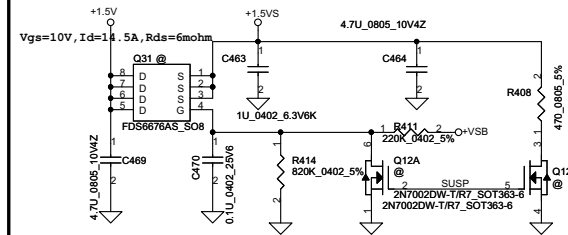
+3VALW TO +3VS



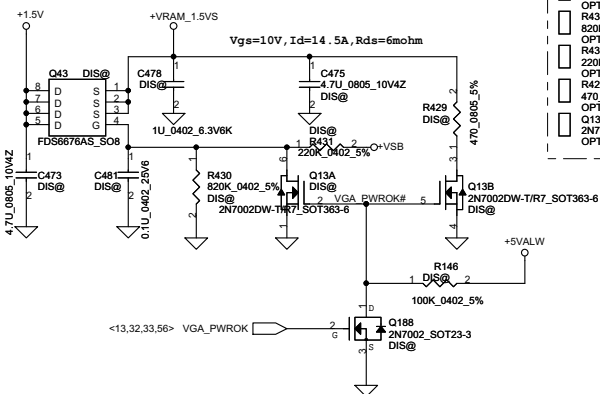
+5VALW TO +5VS



+1.5V to +1.5VS

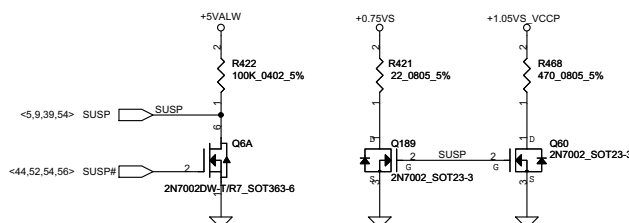
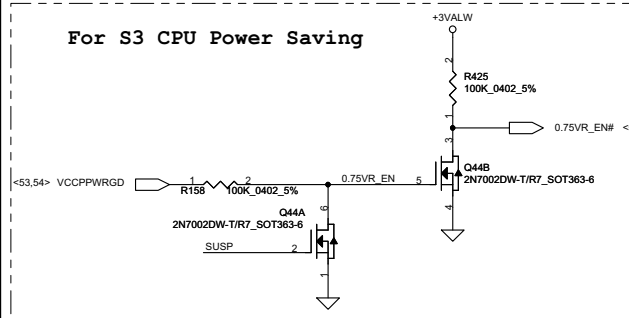


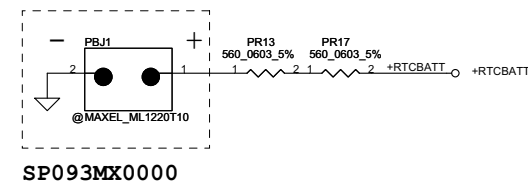
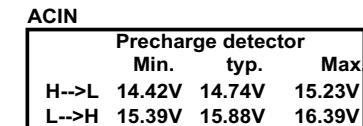
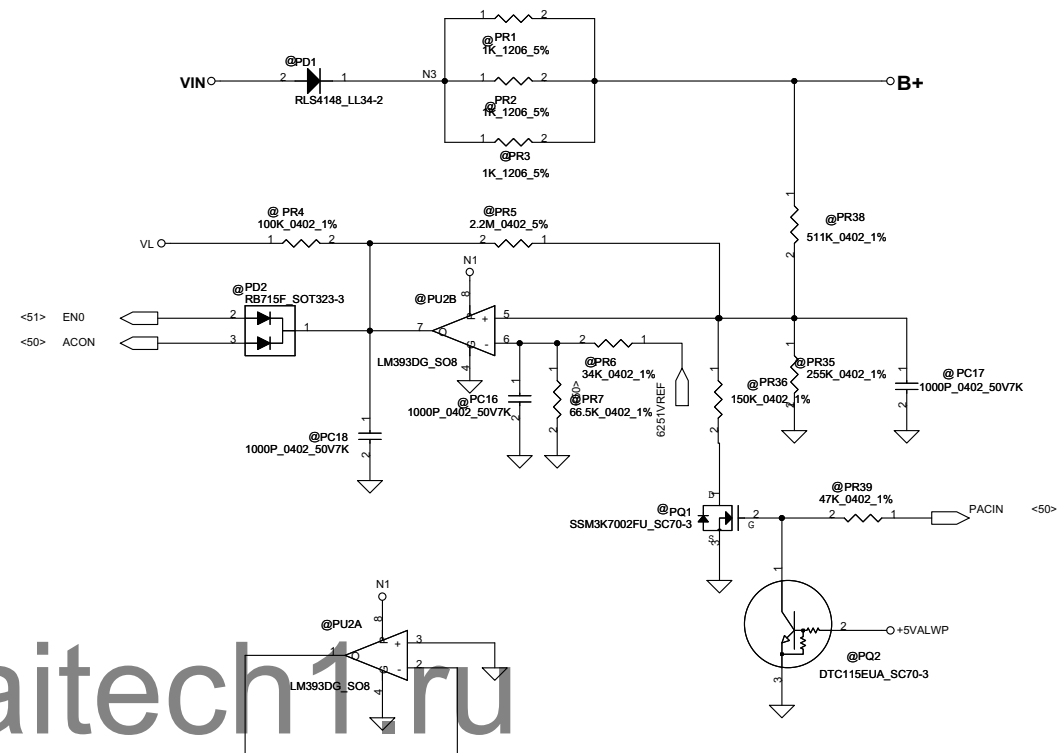
+1.5V to +VRAM_1.5VS



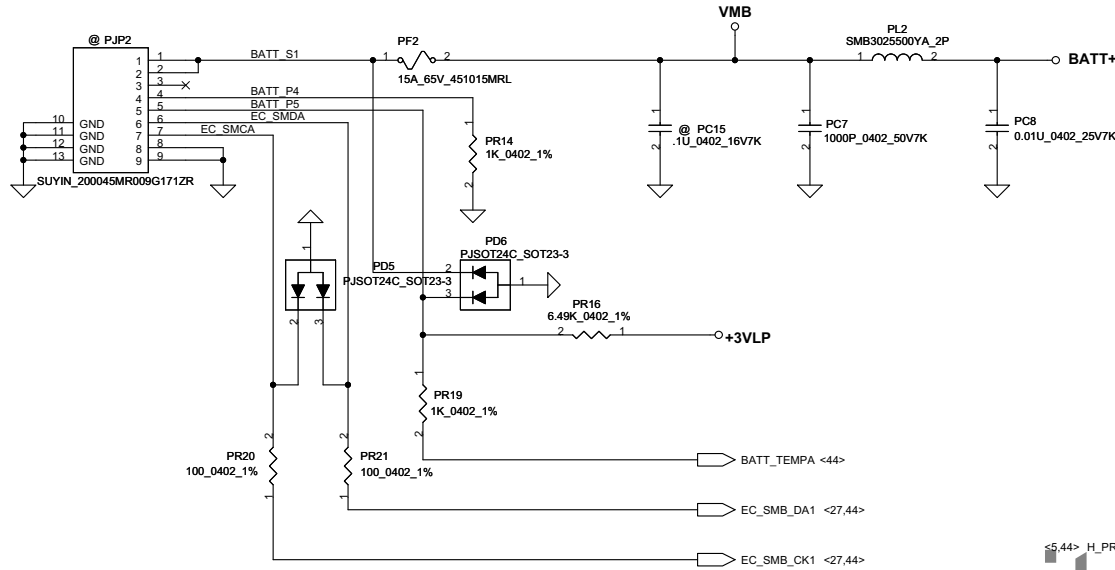
- Q43 FD56676AS_S08 OPT@
- C481 1U_0402_25V6 OPT@
- R430 820K_0402_5% OPT@
- R431 220K_0402_5% OPT@
- R429 470_0805_5% OPT@
- Q13 2N7002DW-T/R7_SOT363-6 OPT@
- C473 47U_0805_10V4Z OPT@
- C478 1U_0402_6.3V6K OPT@
- C475 47U_0805_10V4Z DIS@
- R429 470_0805_5% OPT@
- Q188 2N7002_SOT23-3 DIS@
- Q13 2N7002DW-T/R7_SOT363-6 OPT@

For S3 CPU Power Saving

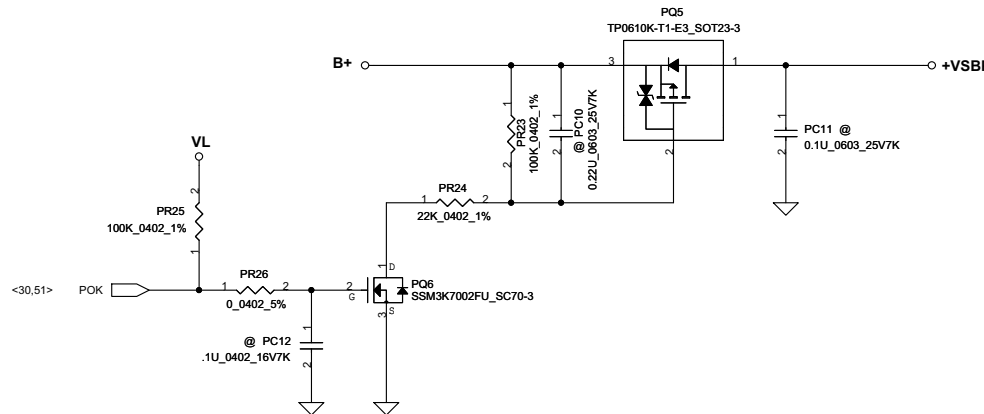
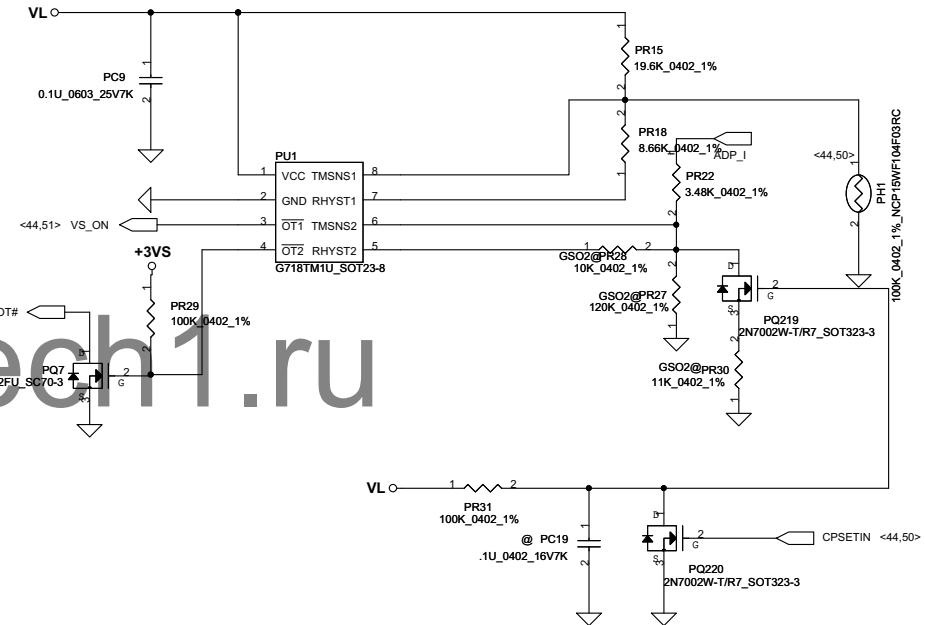




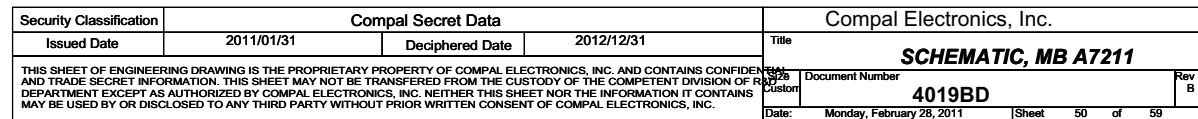
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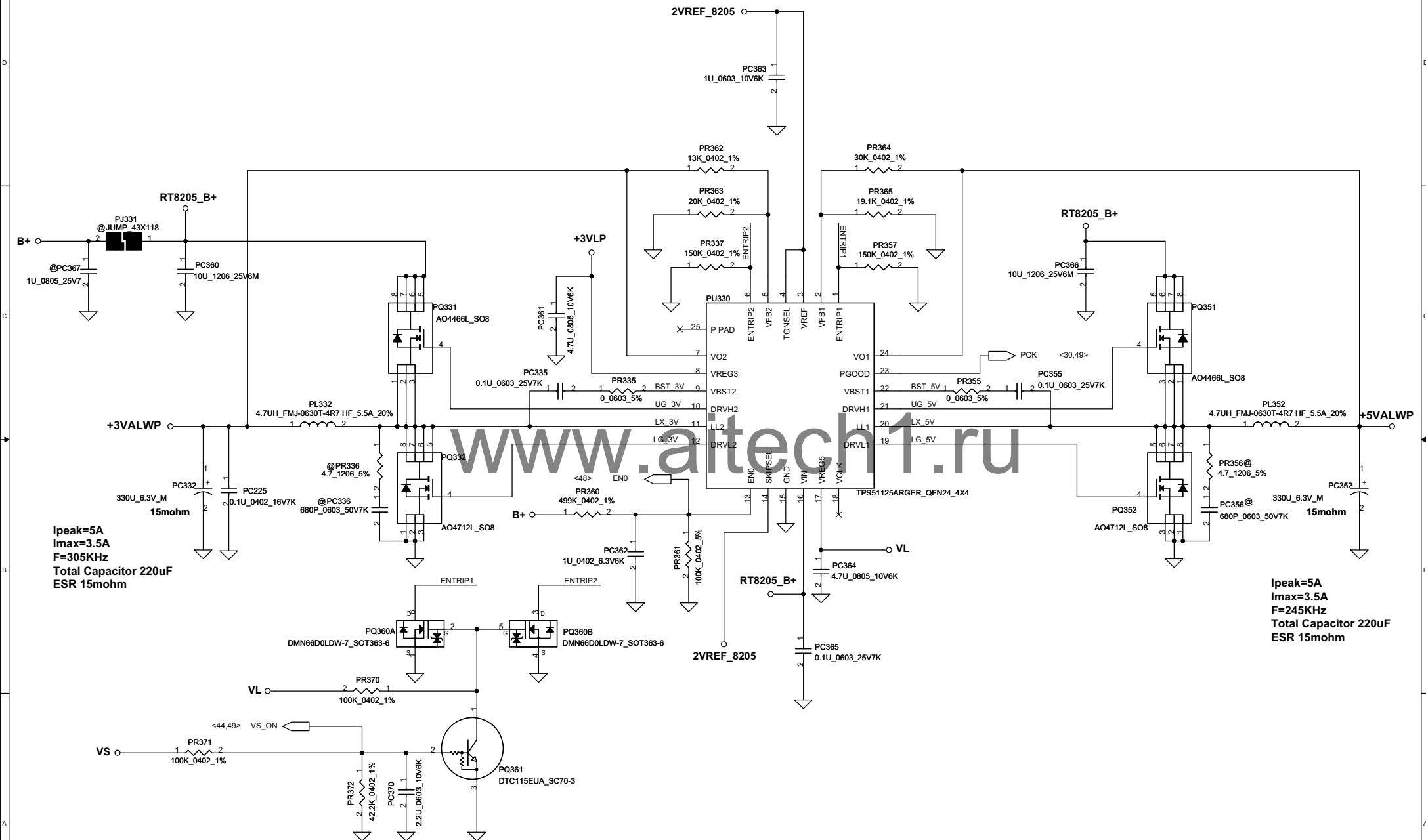


PH1 under CPU bottom side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C

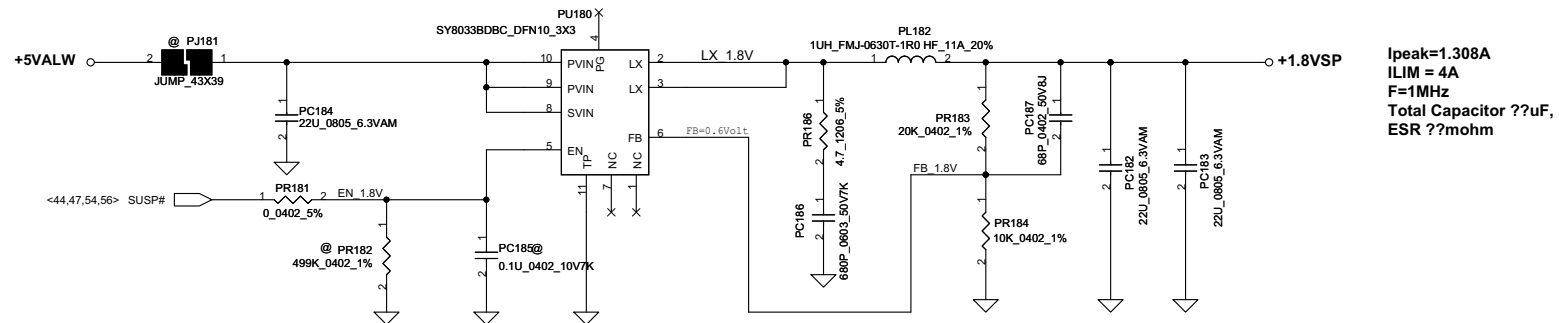


GS2@ PR30 Value = 11K_0402_1% GVO9@ PR30 Value = 14.7K_0402_1%
GS2@ PR28 Value = 10K_0402_1% GVO9@ PR28 Value = 20K_0402_1%
GS2@ PR27 Value = 120K_0402_1% GVO9@ PR27 Value = 15.8K_0402_1%



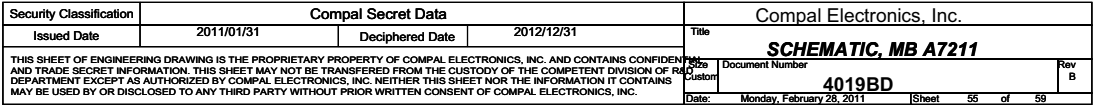


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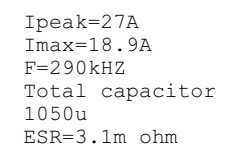


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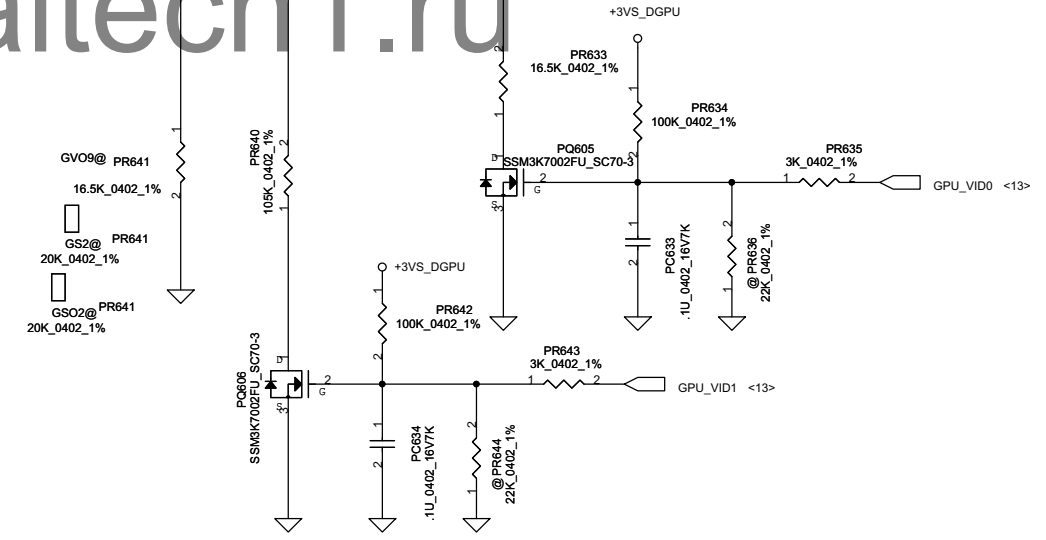
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Pstate	GPU_VID0	GPU_VID1	N12P-GV	N12P-GS
P8/P12	0	0	0.85V	0.825V
P0	1	0	1.0V	0.975V
	0	1		
P0(cold)	1	1	1.025V	1.0V
			PR632=3.57K PR641=16.5K PR633=16.5K PR640=105K	PR632=3.57K PR641=20K PR633=16.5K PR640=105K



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